Dual Very Low Noise Precision Operational Amplifier

OP-270

FEATURES

- **Very Low Noise** ..... **5nV/$\sqrt{Hz}$ @ 1kHz Max**
- **Excellent Input Offset Voltage** ..... **75μV Max**
- **Low Offset Voltage Drift** ..... **1μV/°C Max**
- **Very High Gain** ..... **1500V/mV Min**
- **Outstanding CMR** ..... **106dB Min**
- **Slew Rate** ..... **2.4V/μs Typ**
- **Gain-Bandwidth Product** ..... **5MHz Typ**
- **Industry Standard 8-Pin Dual Pinout**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
75	OP270AZ*	–	OP270ARC/883	MIL
75	OP270EZ	–	–	XIND
150	OP270FZ	–	–	XIND
250	–	OP270GP	–	XIND
250	–	OP270GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

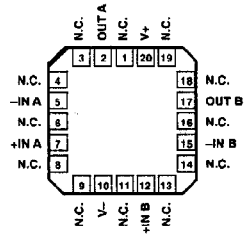
†† For availability and burn-in information on SO and PLCC packages, contact you local sales office.

GENERAL DESCRIPTION

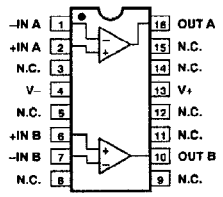
The OP-270 is a high-performance monolithic dual operational amplifier with exceptionally low voltage noise, 5nV/$\sqrt{Hz}$ at 1kHz Max, offering comparable performance to PMI's industry standard OP-27.

The OP-270 features an input offset voltage below 75μV and an offset drift under 1μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP-270 is over 1,500,000 into a 10kΩ load insuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under 20nA which reduces errors due to signal source resistance. The OP-270's CMR of over 106dB and PSRR of less than 3.2μV/V significantly reduce errors due to

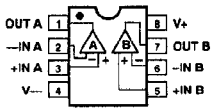
PIN CONNECTIONS



LCC
(RC-Suffix)

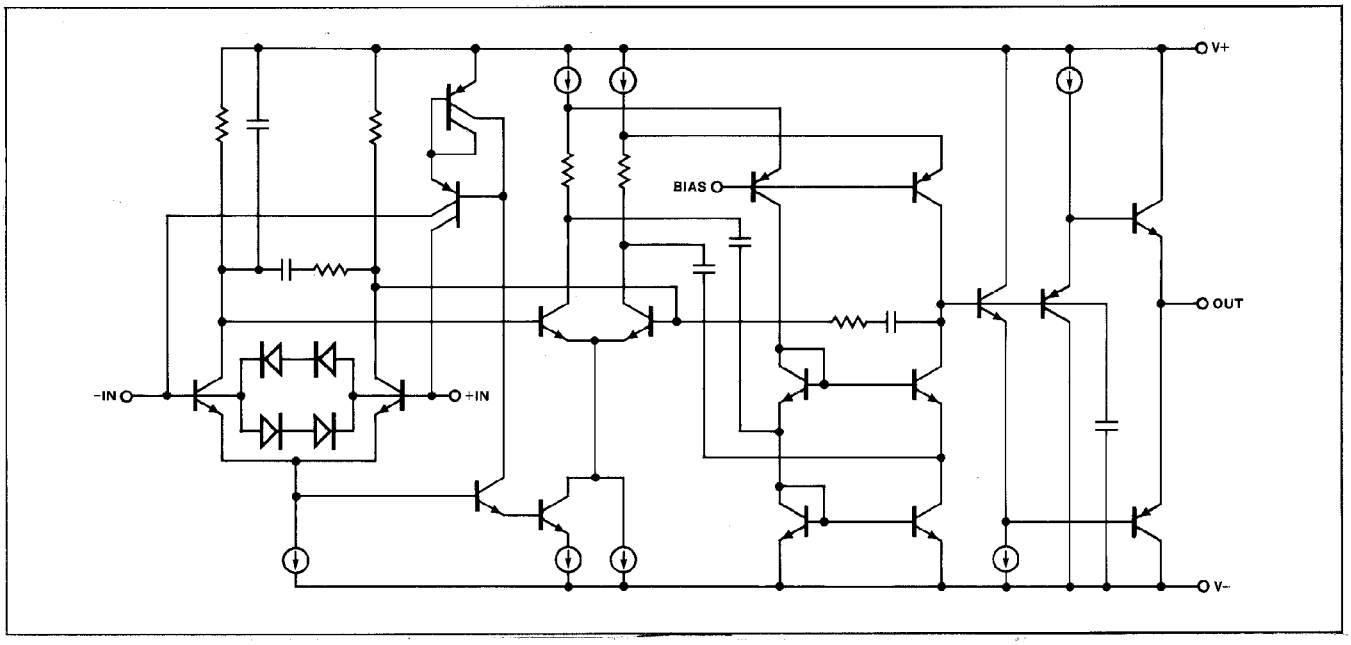


16-PIN SOL
(S-Suffix)



EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



ground noise and power supply fluctuations. Power consumption of the dual OP-270 is one-third less than two OP-27s, a significant advantage for power conscious applications. The OP-270 is unity-gain stable with a gain-bandwidth product of 5MHz and a slew rate of 2.4V/μs.

The OP-270 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, dual buffers, and low-noise active filters.

The OP-270 conforms to the industry standard 8-pin DIP pinout. It is pin compatible with the MC1458/1558, SE5532/A, RM4558 and HA5102 dual op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-271, with a slew rate of 8V/μs, is recommended. For a quad op amp, see the OP-470.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous

Storage Temperature Range
P, RC, S, Z-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C
Operating Temperature Range
OP-270A ..... –55°C to +125°C
OP-270E, OP-270F, OP-270G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-270's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±10V, the input current should be limited to ±25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-270A/E			OP-270F			OP-270G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	–	–	10	75	–	20	150	–	50	250	μV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1	10	–	3	15	–	5	20	nA
Input Bias Current	I_B	V_{CM} = 0V	–	5	20	–	10	40	–	15	60	nA
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz (Note 1)	–	80	200	–	80	200	–	80	–	nVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1kHz (Note 2)	– – –	3.6 3.2 3.2	6.5 5.5 5.0	– – –	3.6 3.2 3.2	6.5 5.5 5.0	– – –	3.6 3.2 3.2	– – –	nV/√Hz
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1kHz	– – –	1.1 0.7 0.6	– – –	– – –	1.1 0.7 0.6	– – –	– – –	1.1 0.7 0.6	– – –	pA/√Hz
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ R_L = 2kΩ	 1500 750	 2300 1200	 – –	 1000 500	 1700 900	 – –	 750 350	 1500 700	 – –	V/mV
Input Voltage Range	IVR	(Note 3)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13.5	–	±12	±13.5	–	±12	±13.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	106	125	–	100	120	–	90	110	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	0.56	3.2	–	1.0	5.6	–	1.5	6	μV/V
Slew Rate	SR		1.7	2.4	–	1.7	2.4	–	1.7	2.4	–	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-270A/E MIN	OP-270A/E TYP	OP-270A/E MAX	OP-270F MIN	OP-270F TYP	OP-270F MAX	OP-270G MIN	OP-270G TYP	OP-270G MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4	6.5	–	4	6.5	–	4	6.5	mA
Gain Bandwidth Product	GBW		–	5	–	–	5	–	–	5	–	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	175	–	125	175	–	–	175	–	dB
Input Capacitance	C_{IN}		–	3	–	–	3	–	–	3	–	pF
Input Resistance Differential-Mode	R_{IN}		–	0.4	–	–	0.4	–	–	0.4	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	20	–	–	20	–	–	20	–	GΩ
Settling Time	t_s	$A_V = +1$, 10V Step to 0.01%	–	5	–	–	5	–	–	5	–	μs

NOTES:
1. Guaranteed by not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for OP-270A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-270A MIN	OP-270A TYP	OP-270A MAX	UNITS
Input Offset Voltage	V_{OS}		–	30	175	μV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	1	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	2	30	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	6	60	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	750 400	1600 800	– –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	–	dB
Power Supply Rejection Ration	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	–	1.0	5.6	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.5	7.5	mA

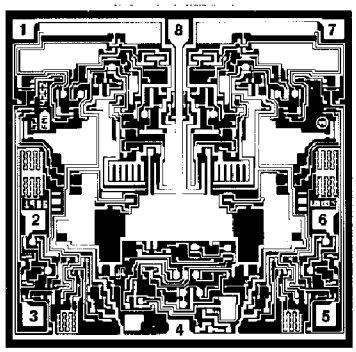
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \leq T_A \leq +85°C$, unless otherwise noted.

			OP-270E			OP-270F			OP-270G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		–	25	150	–	45	275	–	100	400	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	1	–	0.4	2	–	0.7	3	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	1.5	30	–	5	40	–	15	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	6	60	–	15	70	–	19	80	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 1000 500	 1800 900	 – –	 600 300	 1400 700	 – –	 400 225	 1250 670	 – –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	–	94	115	–	90	100	–	dB
Power Supply Rejection Ration	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	–	0.7	5.6	–	1.8	10	–	2.0	15	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.4	7.2	–	4.4	7.2	–	4.4	7.2	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.094 × 0.092 inch, 8,648 sq. mils
(2.39 × 2.34 mm, 5.60 sq. mm)

1. OUT A
2. −IN A
3. +IN A
4. V−
5. +IN B
6. −IN B
7. OUT B
8. V+

Substrate is internally connected to V−.

WAFER TEST LIMITS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

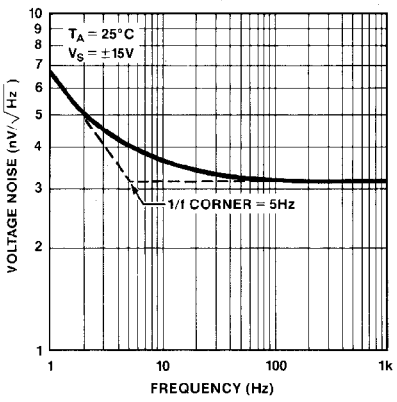
PARAMETER	SYMBOL	CONDITIONS	OP-270G LIMIT	TYP
Input Offset Voltage	V_{OS}		150	µV MAX
Input Offset Current	I_{OS}	V_{CM} = 0V	15	nA MAX
Input Bias Current	I_B	V_{CM} = 0V	40	nA MAX
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	500	V/mV MIN
Input Voltage Range	IVR	(Note 1)	±12	V MIN
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	V MIN
Common-Mode Rejection	CMR	V_{CM} = ±12V	100	dB MIN
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	5.6	µV/V MAX
Supply Current (All Amplifiers)	I_{SY}	No Load	6.5	mA MAX

NOTE:
1. Guaranteed by CMR test.

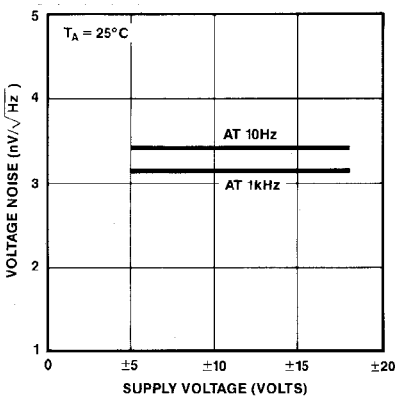
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yields loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

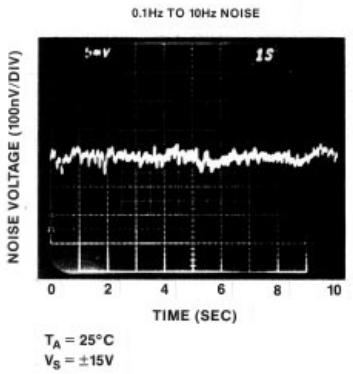
VOLTAGE NOISE DENSITY vs FREQUENCY



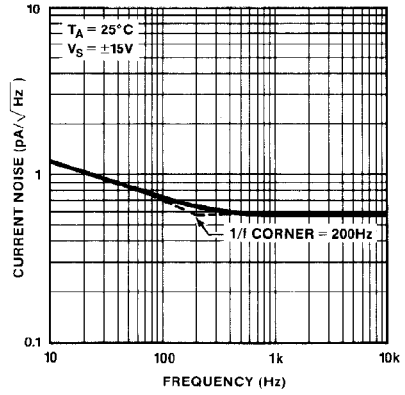
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



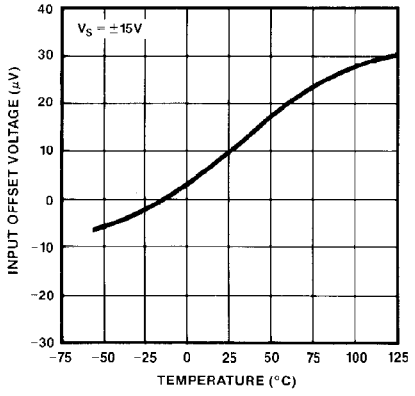
0.1Hz TO 10Hz NOISE



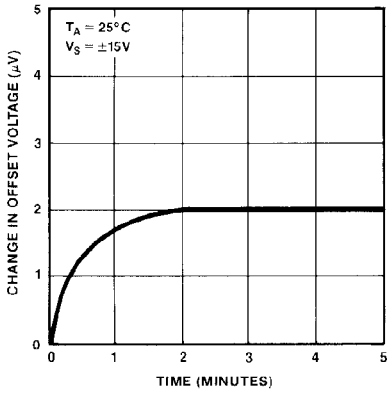
CURRENT NOISE DENSITY vs FREQUENCY



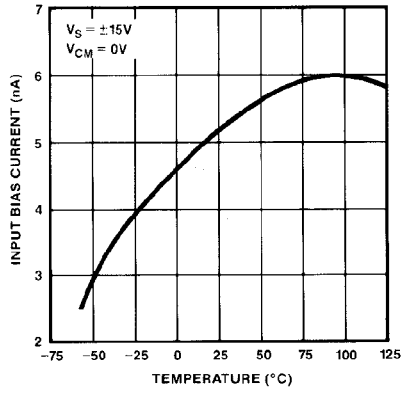
INPUT OFFSET VOLTAGE vs TEMPERATURE



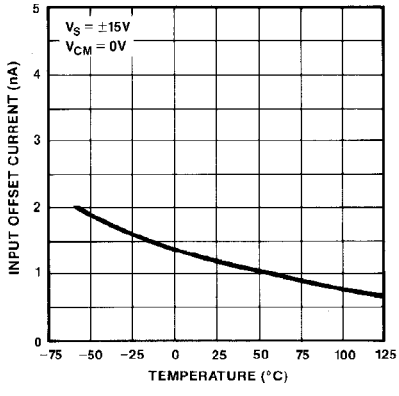
WARM-UP OFFSET VOLTAGE DRIFT



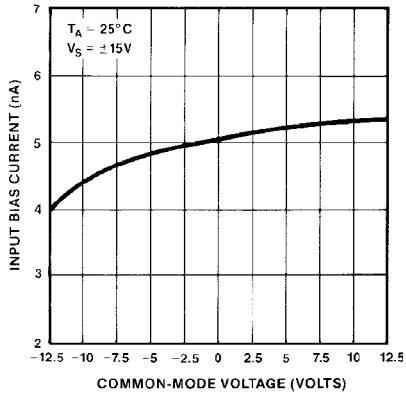
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

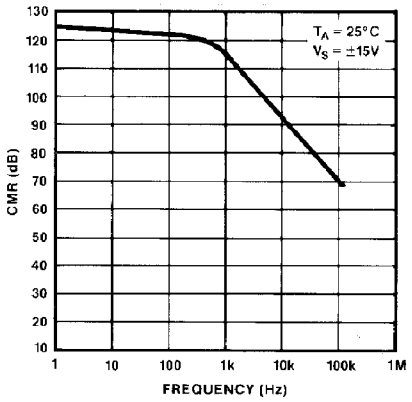


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

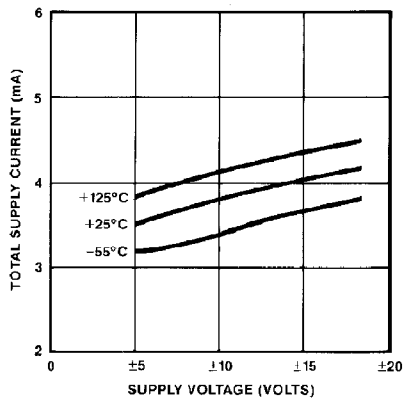


TYPICAL PERFORMANCE CHARACTERISTICS

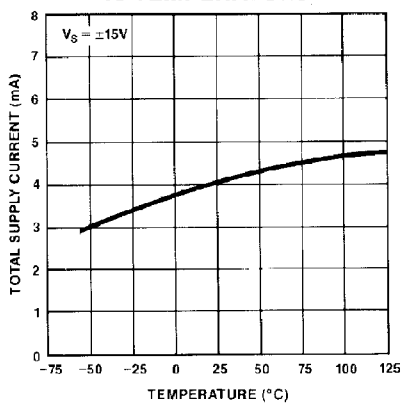
CMR vs FREQUENCY



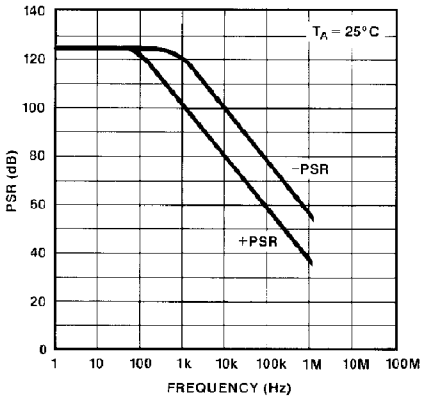
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



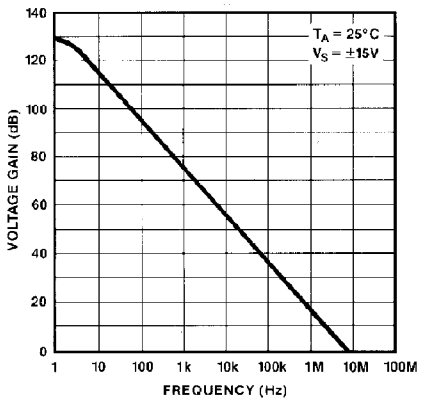
TOTAL SUPPLY CURRENT vs TEMPERATURE



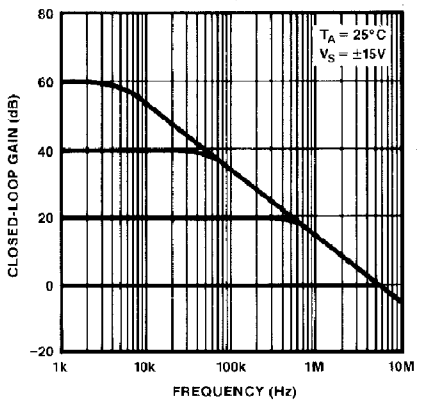
PSR vs FREQUENCY



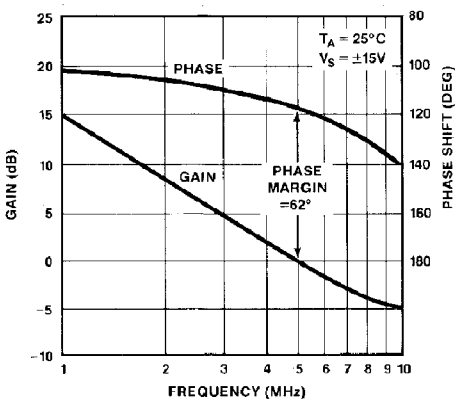
OPEN-LOOP GAIN vs FREQUENCY



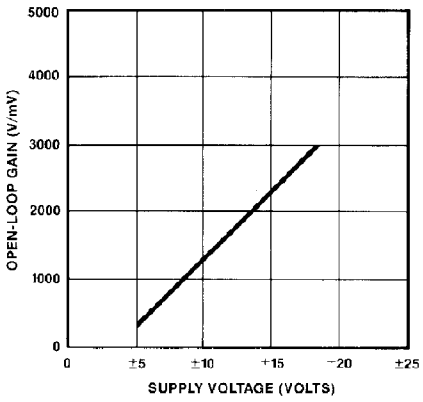
CLOSED-LOOP GAIN vs FREQUENCY



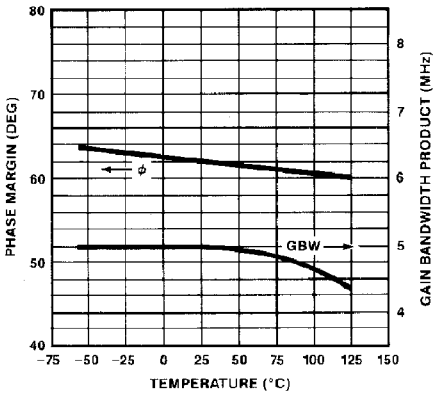
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE



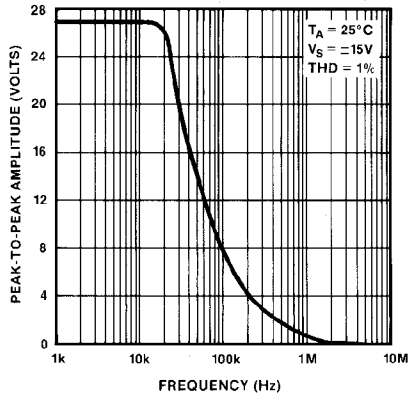
GAIN-BANDWIDTH, PHASE MARGIN vs TEMPERATURE



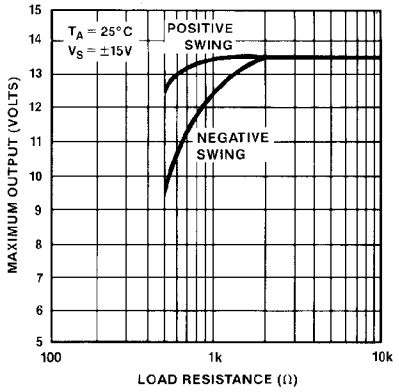
OP-270

TYPICAL PERFORMANCE CHARACTERISTICS

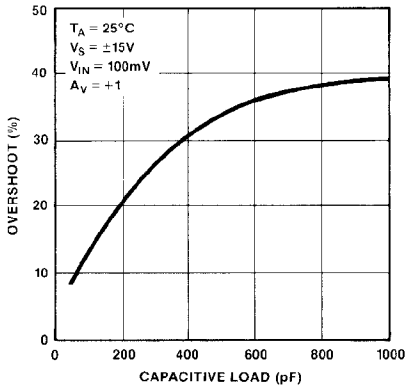
MAXIMUM OUTPUT SWING vs FREQUENCY



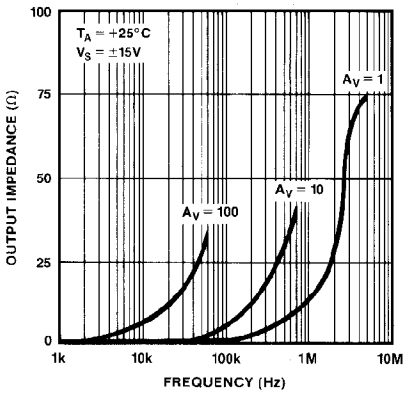
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



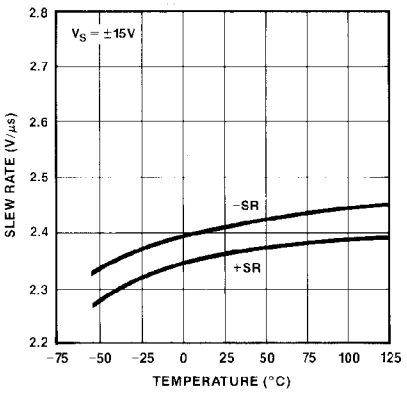
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



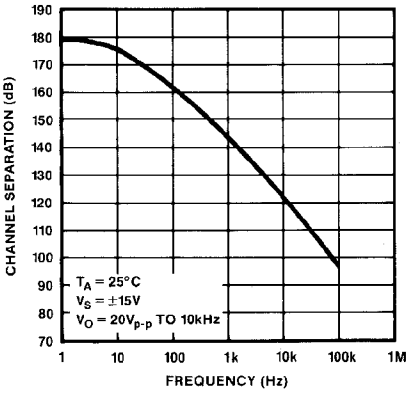
OUTPUT IMPEDANCE vs FREQUENCY



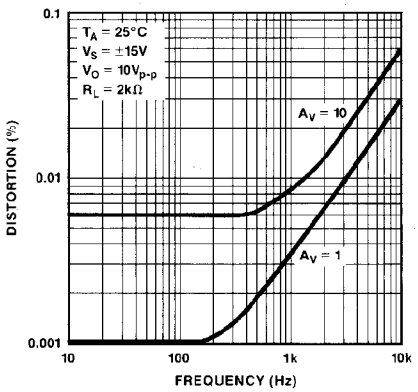
SLEW RATE vs TEMPERATURE



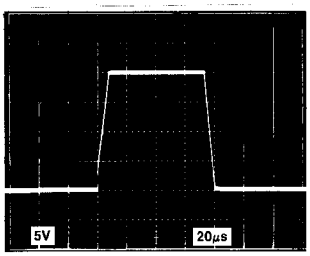
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

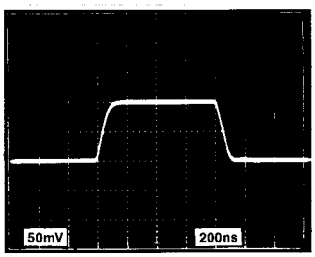


LARGE-SIGNAL TRANSIENT RESPONSE



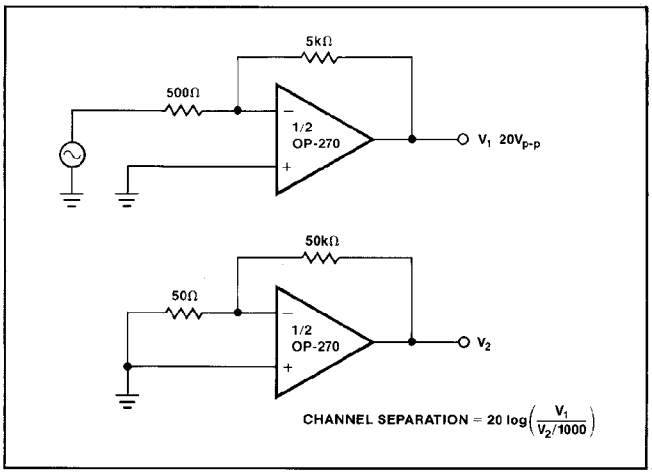
T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 2kΩ

SMALL-SIGNAL TRANSIENT RESPONSE

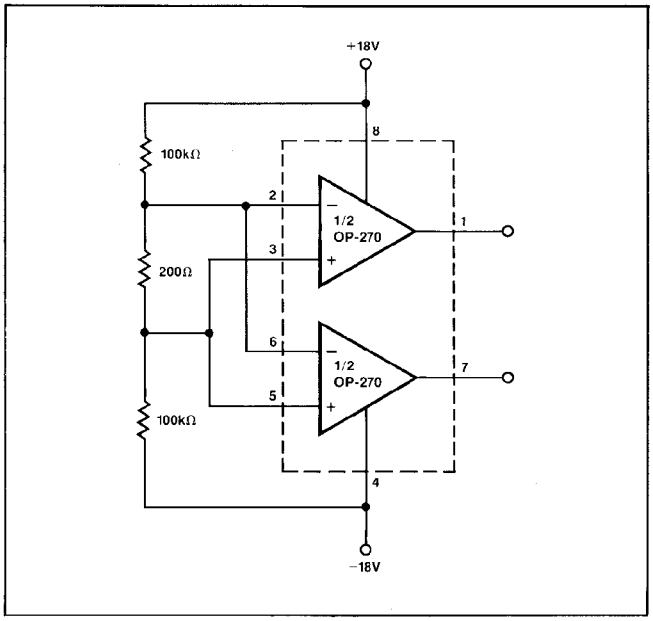


T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 2kΩ

CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP-270 is a very low-noise dual op amp, exhibiting a typical voltage noise of only 3.2nV/√Hz @ 1kHz. The exceptionally low noise characteristics of the OP-270 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-270 is gained at the expense of current noise performance, which is normal for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calculated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1k\Omega$ the total noise is dominated by the voltage noise of the OP-270. As R_S rises above 1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-270. When R_S exceeds 20kΩ, current noise of the OP-270 becomes the major contributor to total noise.

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

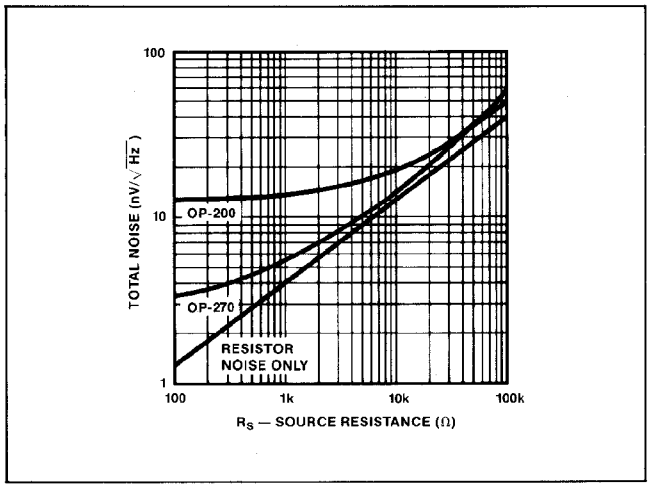


Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-270 dominates the total noise when $R_S > 5k\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-200, with lower current noise than the OP-270, will provide lower total noise.

FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz

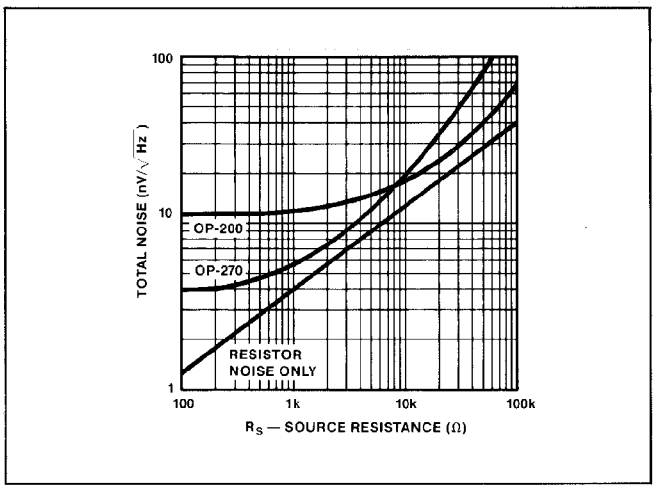


FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)

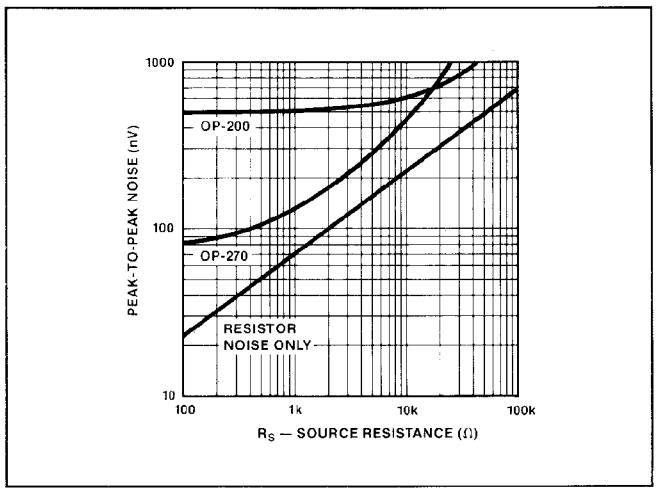


Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the OP-270 is the major contributor to peak-to-peak noise with current noise the major contributor as R_S increases. The crossover point between the OP-270 and the OP-200 for peak-to-peak noise is at $R_S = 17k\Omega$.

The OP-271 is a higher speed version of the OP-270, with a slew rate of 8V/μs. Noise of the OP-271 is slightly higher than the OP-270. Like the OP-270, the OP-271 is unity-gain stable.

For reference, typical source resistances of some signal sources are listed in Table 1.

TABLE 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead, microphone	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-270 I_B can be neglected.
Magnetic phonograph cartridge	<1500Ω	Similar need for low I_B in direct coupled applications. OP-270 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 200nV peak-to-peak noise specification of the OP-270 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 2μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts

FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)

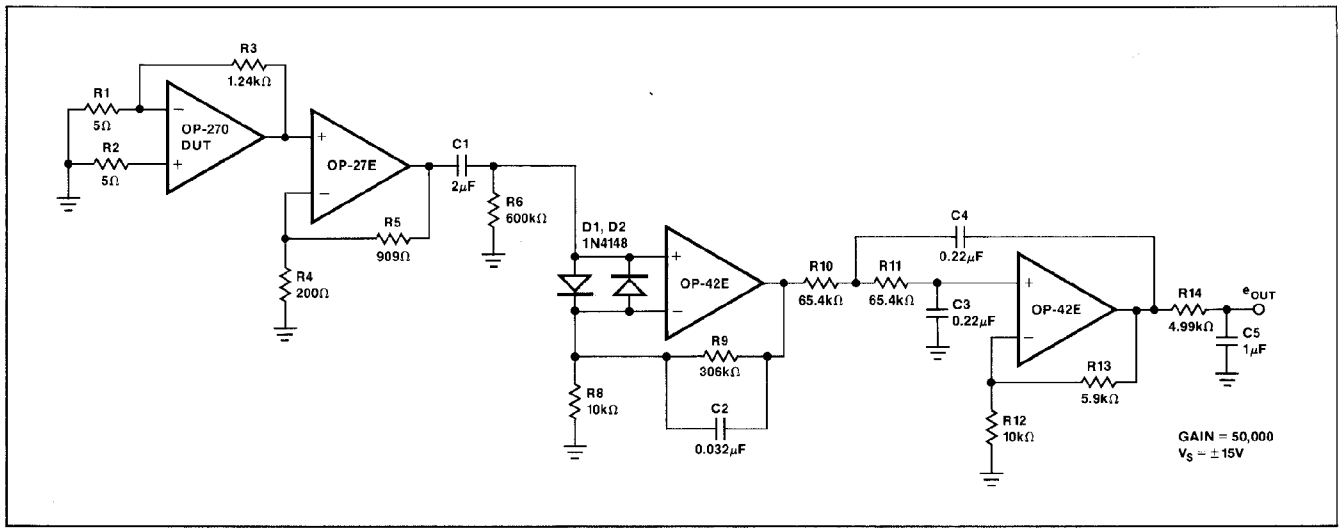
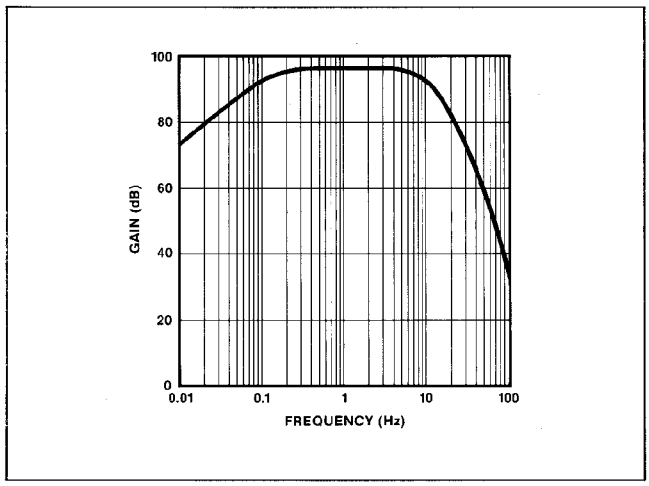


FIGURE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.

5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced via the amplifier supply pins.

NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of dual op amps. The first amplifier is in unity-gain, with the final amplifier in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101 \left(\sqrt{e_{nA}^2 + e_{nB}^2} \right)$$

The OP-270 is a monolithic device with two identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101 \left(\sqrt{2e_n^2} \right) = 101 \left(\sqrt{2}e_n \right)$$

FIGURE 6: Noise Voltage Density Test Circuit

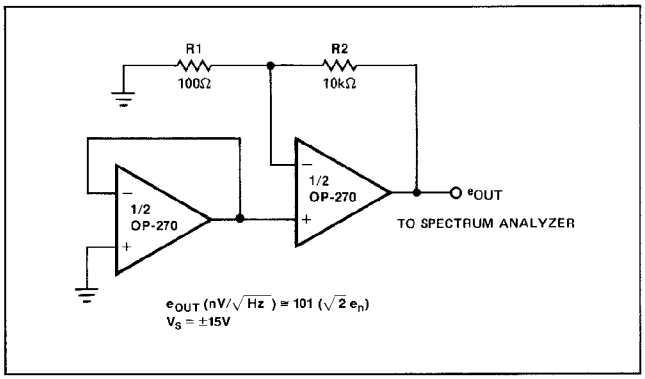
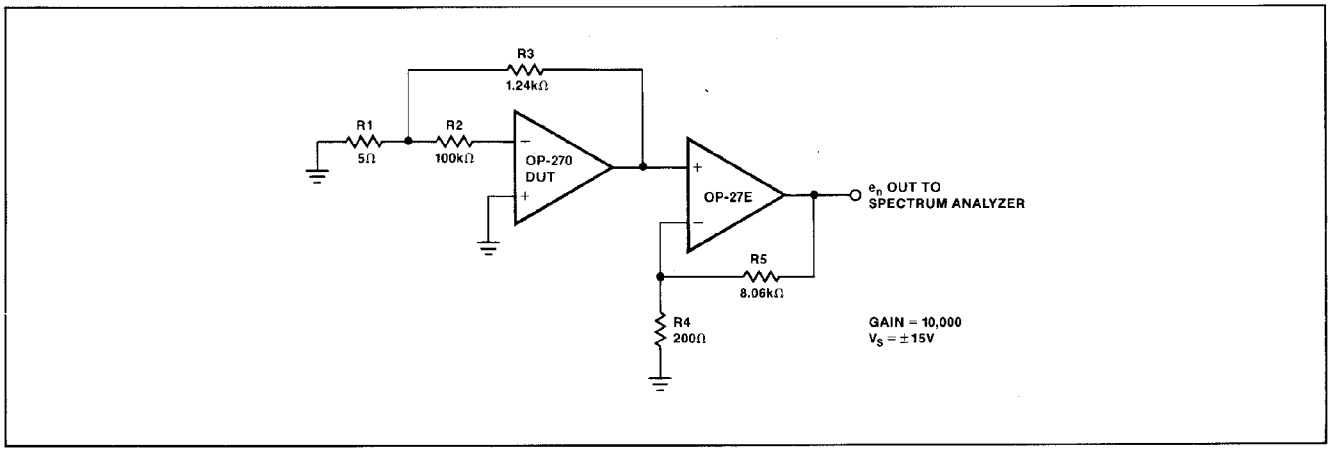


FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

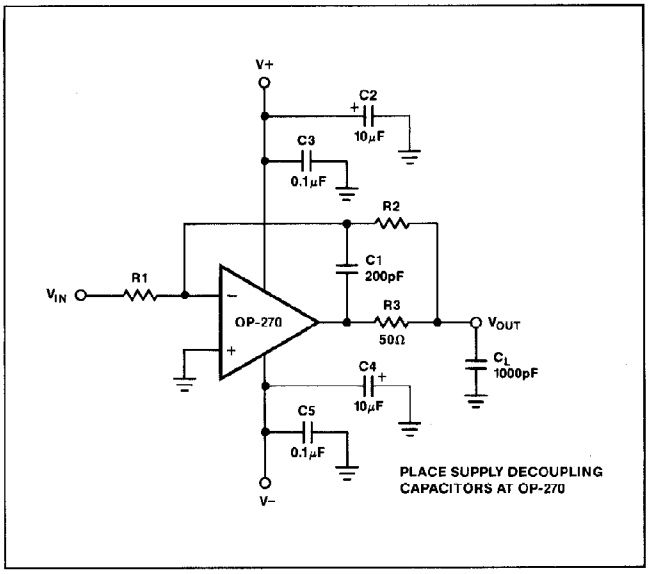
G = gain of 10000
R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-270 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-270.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-270.

FIGURE 8: Driving Large Capacitive Loads



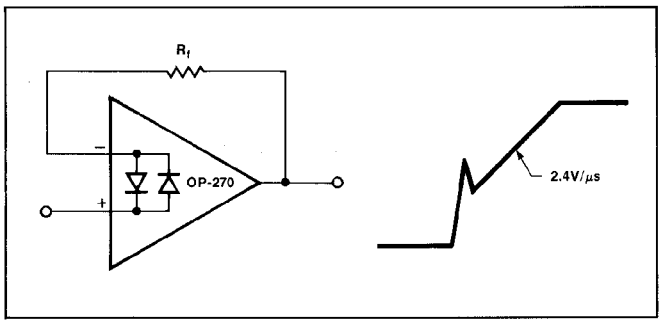
UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L < 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (3pF) creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f helps eliminate this problem.

FIGURE 9: Pulsed Operation



APPLICATIONS

LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 10 utilizes a monolithic dual operational amplifier and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $V_O/(K1 + 1) = V_2/(K1 + 1)$ yielding an overall transfer function of $V_O/V_{IN} = K1 + 1$. The DC gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note, that like a conventional single op amp amplifier, the DC gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

FIGURE 10: Low Phase Error Amplifier

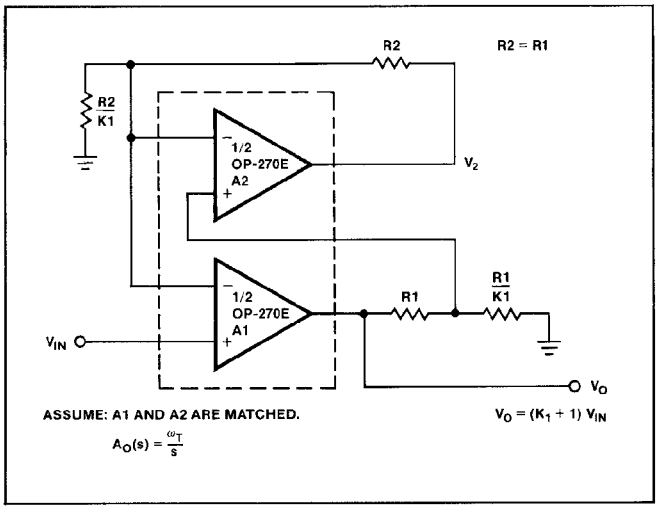


Figure 11 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of −0.1° occurs at 0.002 $\omega/\beta\omega_T$ for the single op amp amplifier, but at 0.11 $\omega/\beta\omega_T$ for the low phase error amplifier.

For more detailed information on the low phase error amplifier, see Application Note AN-107.

FIGURE 11: Phase Error Comparison

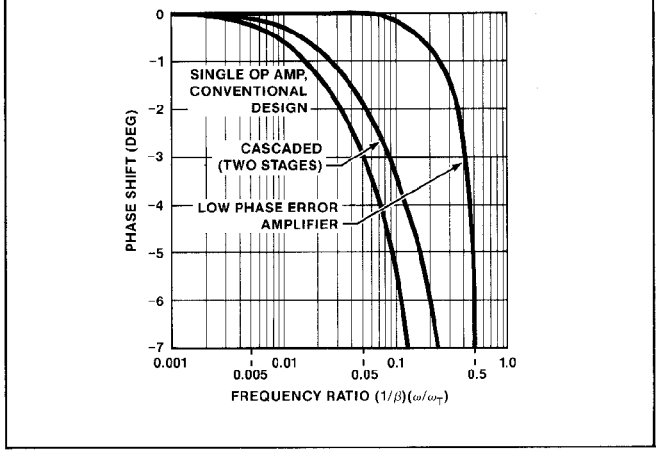
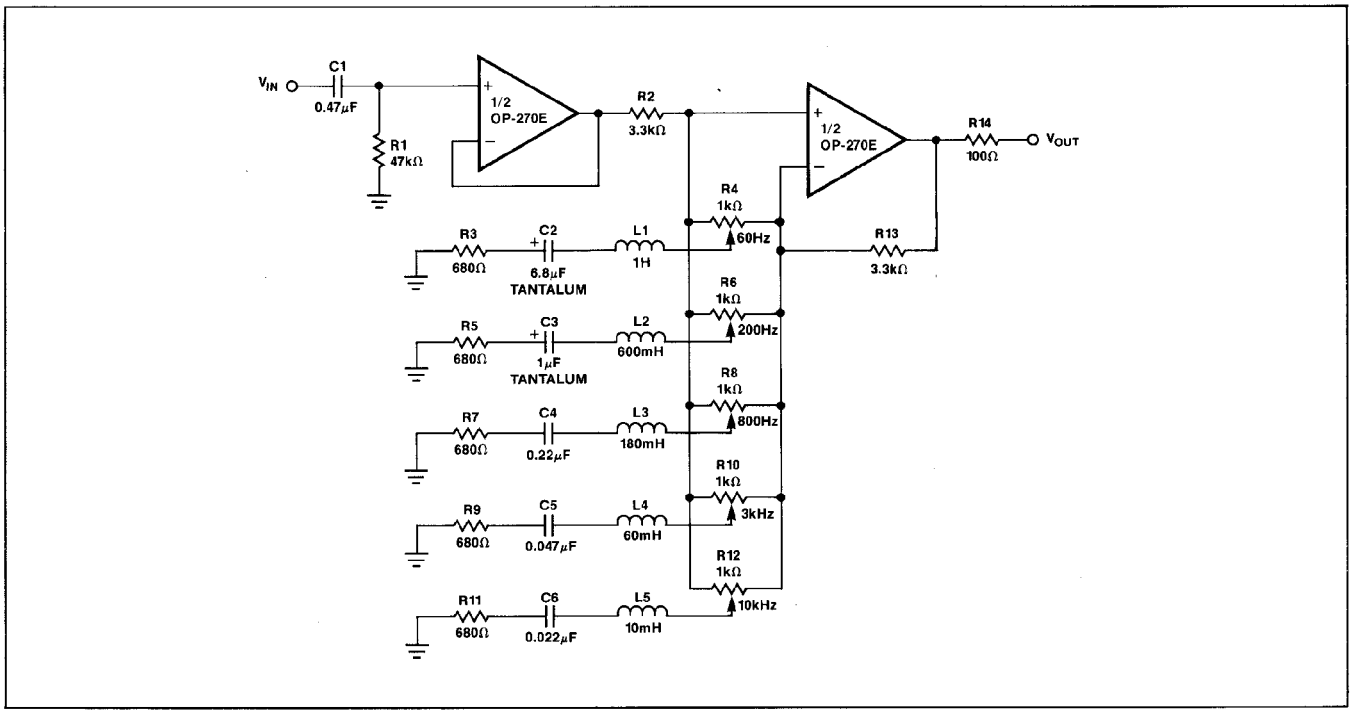


FIGURE 12: 5-Band Low Noise Graphic Equalizer



FIVE-BAND LOW NOISE STEREO GRAPHIC EQUALIZER

The graphic equalizer circuit shown in Figure 12 provides 15dB of boost or cut over a 5-band range. Signal-to-noise ratio over a 20kHz bandwidth is better than 100dB referred to a 3V rms input. Larger inductors can be replaced by active inductors but this reduces the signal-to-noise ratio.

DIGITAL PANNING CONTROL

Figure 13 uses a DAC-8221, a dual 12-bit CMOS DAC, to pan a signal between two channels. One channel is formed by the current output of DAC A driving one-half of an OP-270 in a current-to-voltage converter configuration. The other channel is formed by the complementary output current of DAC A which normally flows to ground though the AGND pin. This complementary current is converted to a voltage by the other half of the OP-270 which also holds AGND at virtual ground.

Gain error due to mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resistors is eliminated by using feedback resistors internal to the DAC-8221. Only DAC A passes a signal; DAC B provides the second feedback resistor. With $V_{REF}B$ unconnected, the current-to-voltage converter, using $R_{FB}B$, is accurate and not influenced by digital data reaching DAC B. Distortion of the digital panning control is less than 0.002% over the 20Hz-20kHz audio range. Figure 14 shows the complementary outputs for a 1kHz input signal and a digital ramp applied to the DAC data input.

DUAL PROGRAMMABLE GAIN AMPLIFIER

The dual OP-270 and the DAC-8221, a dual 12-bit CMOS DAC, can be combined to form a space-saving dual programmable amplifier. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the internal feedback resistor and the resistance the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{4096}{n}$$

where n equals the decimal equivalent of the 12-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will open causing the op amp output to saturate. A 20MΩ resistor placed in parallel with the DAC feedback loop eliminates this problem with only a very small reduction in gain accuracy.

FIGURE 13: Digital Panning Control

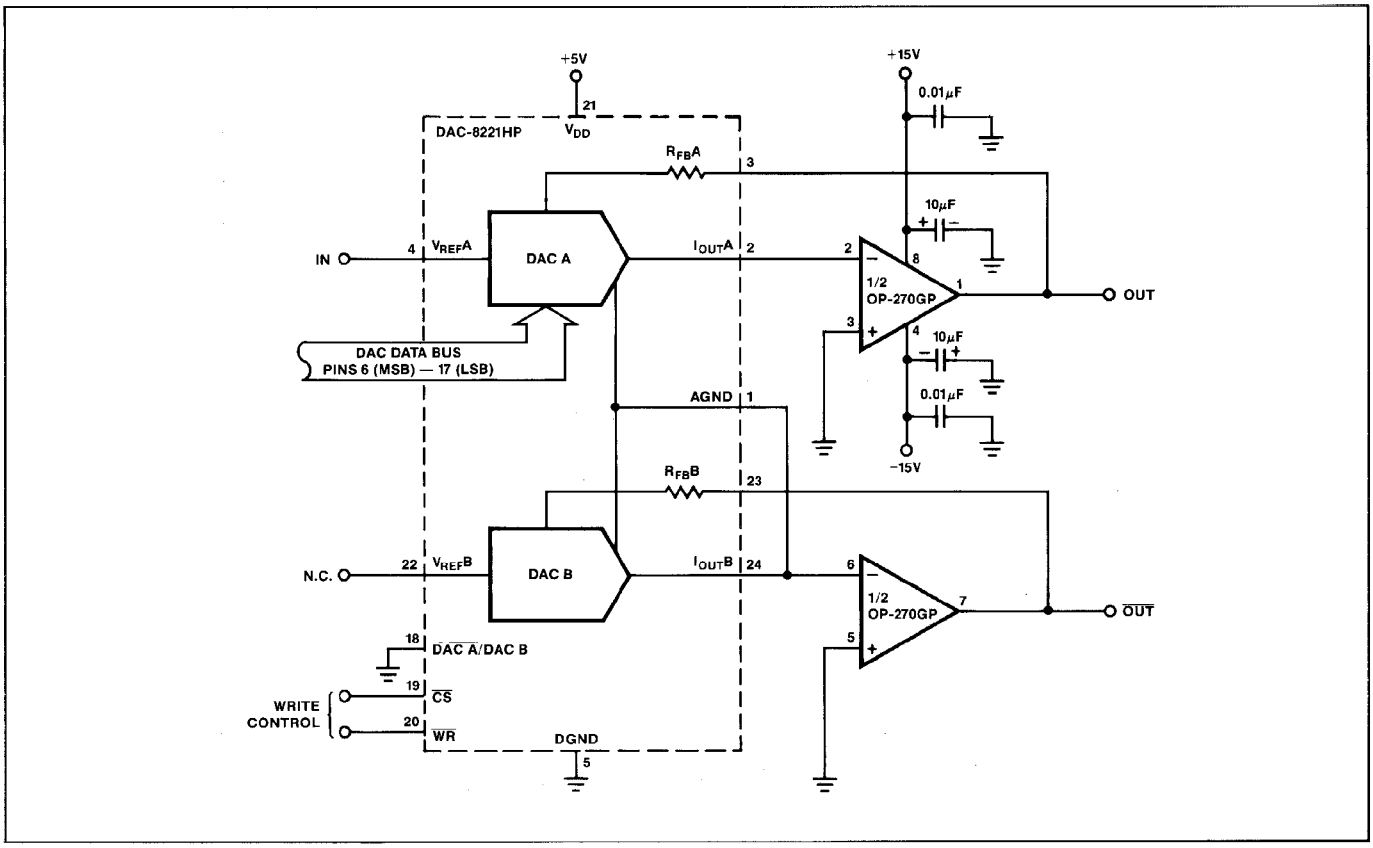


FIGURE 14: Digital Panning Control Output

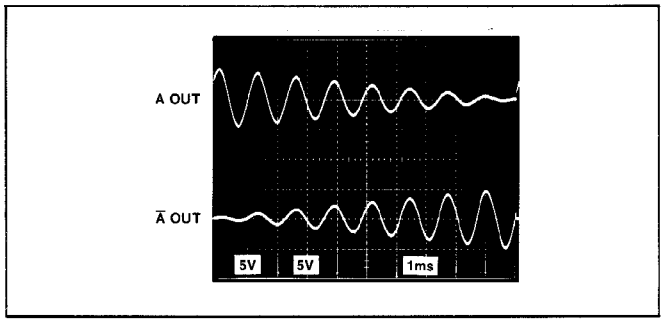


FIGURE 15: Dual Programmable Gain Amplifier

