

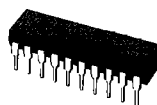
OCTAL D FLIP-FLOP WITH COMMON ENABLE AND CLOCK

- 8-BIT HIGH SPEED PARALLEL REGISTERS
- POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOP
- FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

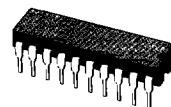
DESCRIPTION

The T54LS377 is an 8-Bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable. The device is packaged in the spacesaving (0.3 inch row spacing) 20 pin package.

E	Enable (Active LOW) Input
D ₀ -D ₇	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
Q ₀ -Q ₇	True Outputs



B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

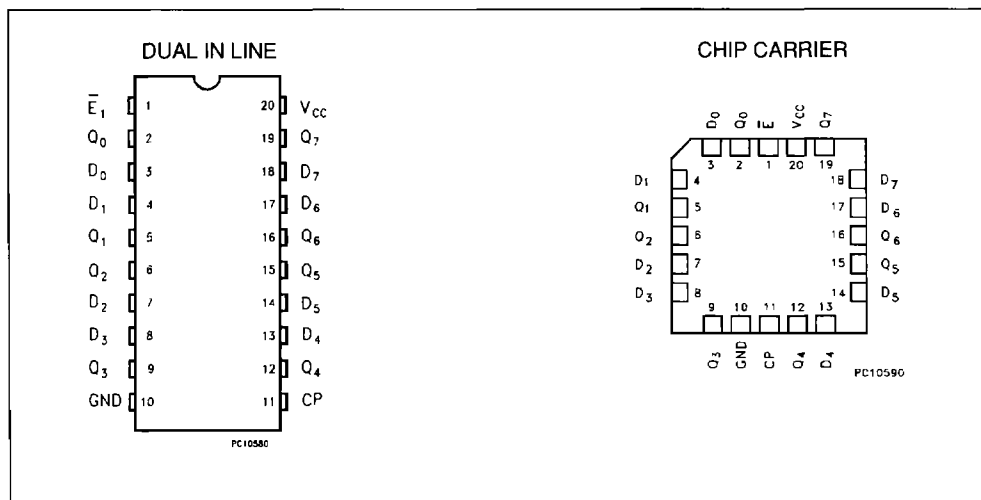


C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS377 D1 T74LS377 C1
 T74LS377 B1 T74LS377 M1

PIN CONNECTION (top view)



TRUTH TABLE

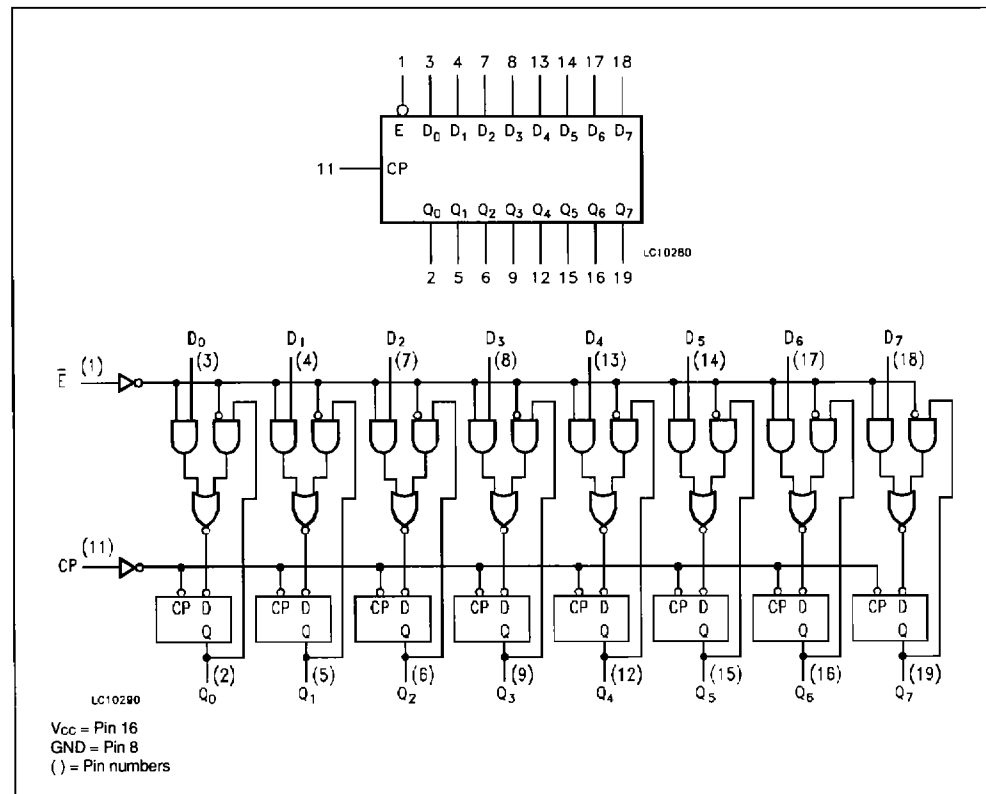
E	CP	D _n	Q _n
H		X	No Change
L		H	H
L		L	L

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

LOGIC SYMBOL AND LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS377 consists of eight edge-triggered D flip-flop with individual D inputs and Q outputs. The Clock (CP) and Enable input ($\bar{E}$) are common to all flip-flop.

When $\bar{E}$ is LOW, new data is entered into the register on the next LOW to HIGH transition of (CP).

When $\bar{E}$ is HIGH, the register will retain the present data independent of the CP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	- 0.5 to + 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to + 10	V
I_I	Input Current, Into Inputs	- 30 to + 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS377XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for all Inputs	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	V
V_{OH}	Output HIGH Voltage	2.5	3.5		$V_{CC} = \text{MIN}$, $I_{OH} = - 400 \mu\text{A}$ $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	V
V_{OL}	Output LOW Voltage		0.25	0.4	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
			0.35	0.5	$I_{OL} = 8.0 \text{ mA}$	V
I_{IH}	Input HIGH Current			20 0.1	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$ $V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	μA mA
I_{IL}	Input LOW Current			- 0.4	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	$V_{CC} = \text{MAX}$, $V_{OUT} = 0 \text{ V}$	mA
I_{CC}	Power Supply Current		18	28	$V_{CC} = \text{MAX}$	mA

Notes : 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

2) Not more than one output should be shorted at a time.

(*) Typical values are at $V_{CC} = 5.0 \text{ V}$, $T_A = 25 \text{ °C}$.

AC CHARACTERISTICS: $T_A = 25 \text{ °C}$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	30	40		Figures 1	MHz
t_{PLH}	Propagation Delay, Clock to Outputs		17	27	Figures 1	ns
t_{PHL}	Propagation Delay, Clock to Outputs		18	27	Figures 1	ns

$V_{CC} = 5.0 \text{ V}$
 $C_L = 15 \text{ pF}$
 $R_L = 2 \text{ K}\Omega$

AC SET-UP REQUIREMENTS: $T_A = 25\text{ }^{\circ}\text{C}$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
$t_w(\text{CP})$	Minimum Clock Pulse Width	20			Figure 1	ns
t_s	Set-Up Time, Data to Clock (HIGH or LOW)	20			Figure 1	ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Figure 1	ns
t_{sH}	Set-Up Time HIGH Enable to Clock	10			Figure 1	ns
t_{hH}	Hold Time HIGH Enable to Clock	5			Figure 1	ns
t_{sL}	Set-Up Time LOW Enable to Clock	25			Figure 1	ns
t_{hL}	Hold Time LOW Enable to Clock	5			Figure 1	ns

$V_{CC} = 5.0\text{ V}$
 $C_L = 15\text{ pF}$
 $R_L = 2\text{ K}\Omega$

DEFINITION OF TERMS:

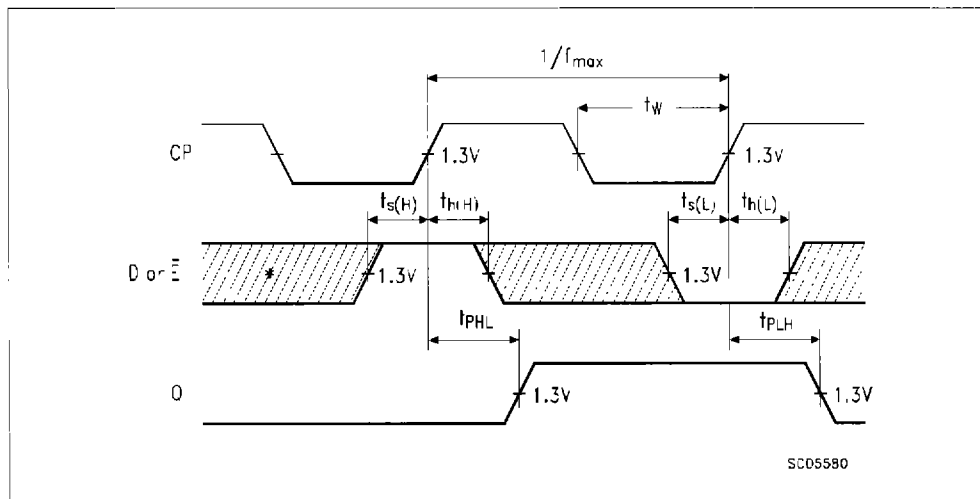
SET-UP TIME (t_s): is defined as the minimum time required for the correct logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time fol-

lowing the clock transition from LOW to HIGH at which the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relaxed prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS

Figure 1: Clock to Output Delays, Clock Pulse Width, Frequency Set-up and Hold Times Data to Clock



* The shaded areas indicate when the input is permitted to change for predictable output performance