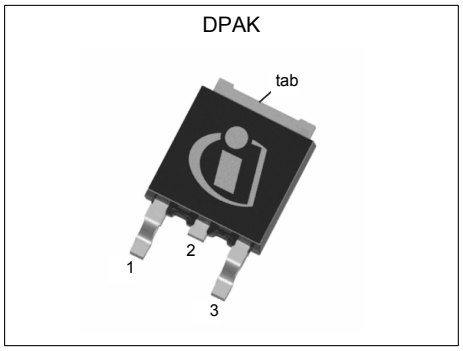
MOSFET

OptiMOS™3 Power-Transistor, 30 V



Features

- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC[1] for target applications
- N-channel, logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Avalanche rated
- Pb-free plating
- Halogen-free according to IEC61249-2-21
- Avalanche rated
- Pb-free plating; RoHS compliant

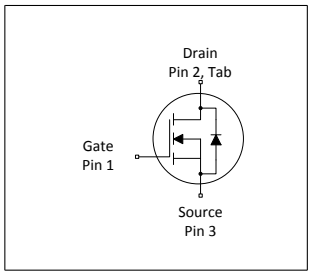


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	6	mΩ
I_D	50	A

Type / Ordering Code	Package	Marking	Related Links
IPD060N03L G	PG-TO252-3	060N03L	-

[1] J-STD20 and JESD22

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - - -	- - - -	50 50 50 43	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C
Pulsed drain current[1]	$I_{D,pulse}$	-	-	350	A	T_C=25 °C
Avalanche current, single pulse[2]	I_{AS}	-	-	50	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	60	mJ	I_D=20 A, R_{GS}=25 Ω
Reverse diode dv/dt	dv/dt	-	-	6	kV/µs	I_D=50 A, V_{DS}=24 V, di/dt=200 A/µs, $T_{j,max}$=175 °C
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	56	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.7	K/W	-
SMD version, device on PCB, minimal footprint	R_{thJA}	-	-	75	K/W	-
SMD version, device on PCB, 6 cm² cooling area[3]	R_{thJA}	-	-	50	K/W	-

[1] See figure 3 for more detailed information
[2] See figure 13 for more detailed information
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1	-	2.2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance[1]	$R_{DS(on)}$	- -	7.2 5	9 6	mΩ	V_{GS}=4.5 V, I_D=30 A V_{GS}=10 V, I_D=30 A
Gate resistance	R_G	-	1.4	-	Ω	-
Transconductance	g_{fs}	34	67	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[2]	C_{iss}	-	1700	2300	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance[2]	C_{oss}	-	640	850	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance[2]	C_{rss}	-	35	52	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	5	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω
Rise time	t_r	-	3	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	20	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω
Fall time	t_f	-	3	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω

Table 6 Gate charge characteristics[3]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5.6	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	2.8	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	2.5	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	5.3	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[2]	Q_g	-	10.8	14.4	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	3.2	-	V	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[2]	Q_g	-	22	30	-	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	9.4	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge	Q_{oss}	-	17	-	-	V_{DD}=15 V, V_{GS}=0 V

[1] Measured from drain tab to source pin
[2] Defined by design. Not subject to production test
[3] See ″Gate charge waveforms″ for parameter definition

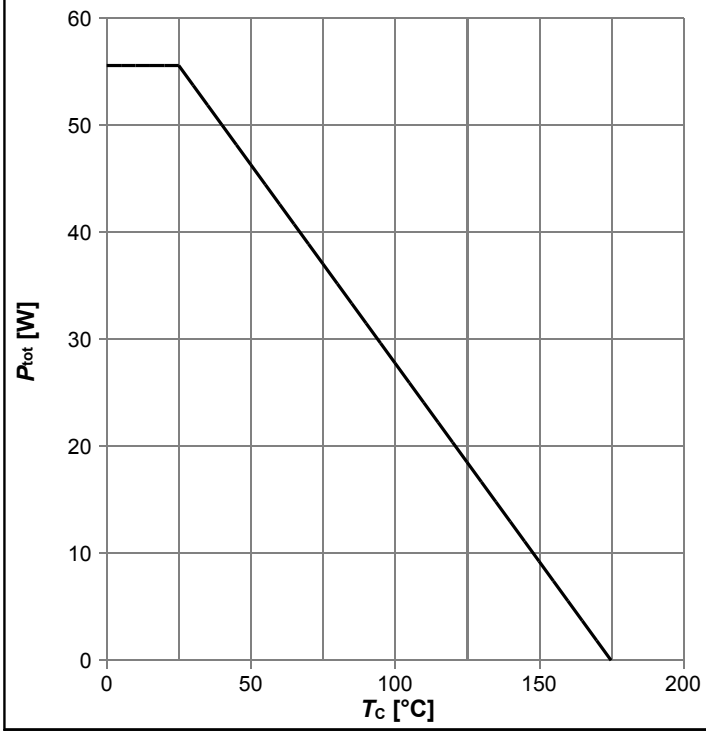
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	50	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	350	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.88	1.1	V	V_{GS}=0 V, I_F=30 A, T_j=25 °C
Reverse recovery charge[1)]	Q_{rr}	-	-	10	nC	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs

[1)] Defined by design. Not subject to production test

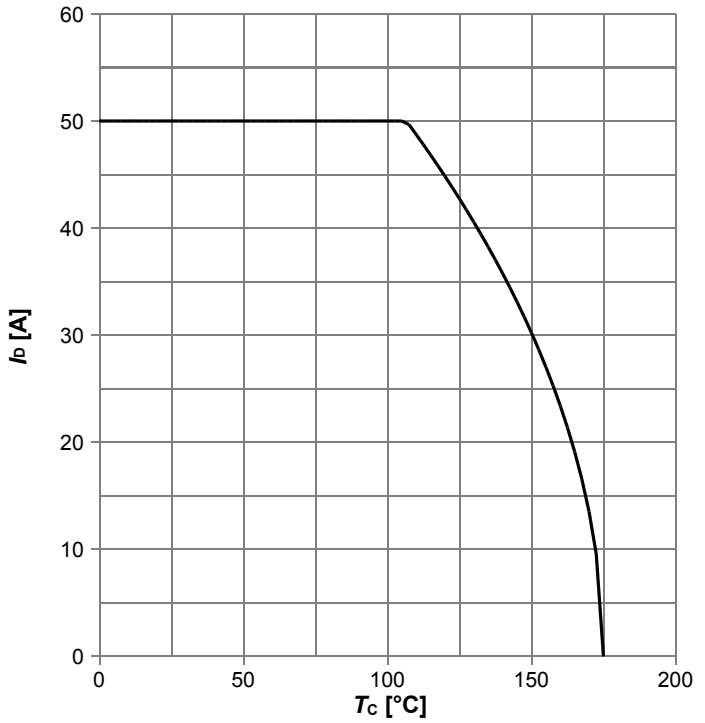
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



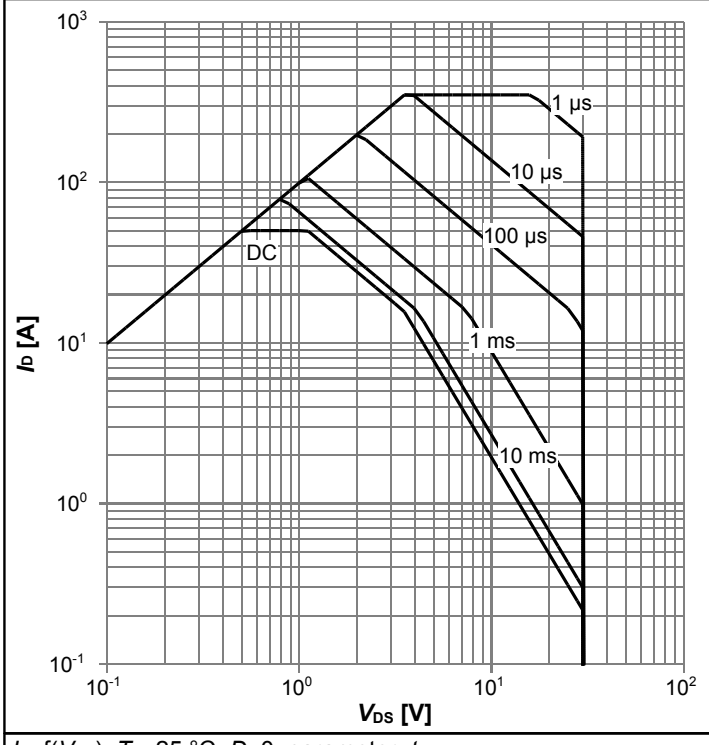
$P_{tot}=f(T_C)$

Diagram 2: Drain current



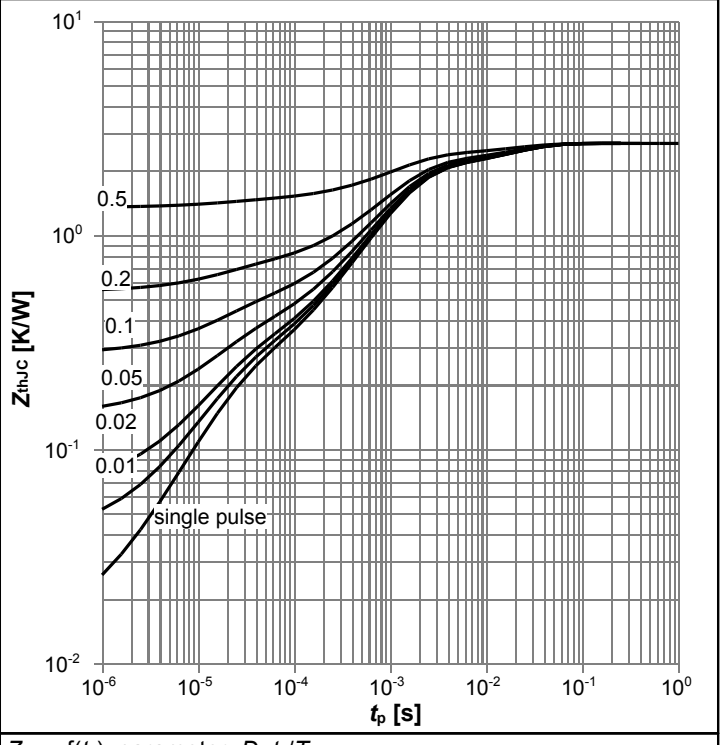
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



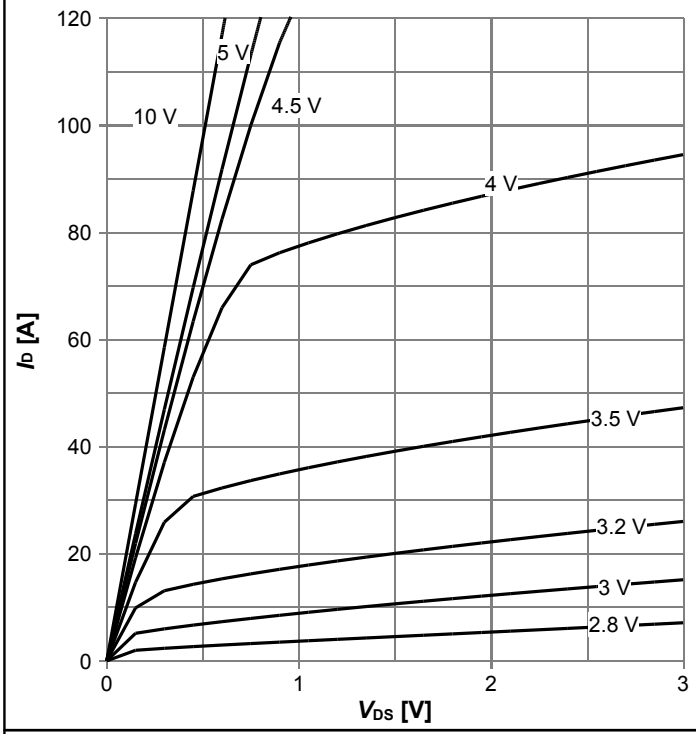
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



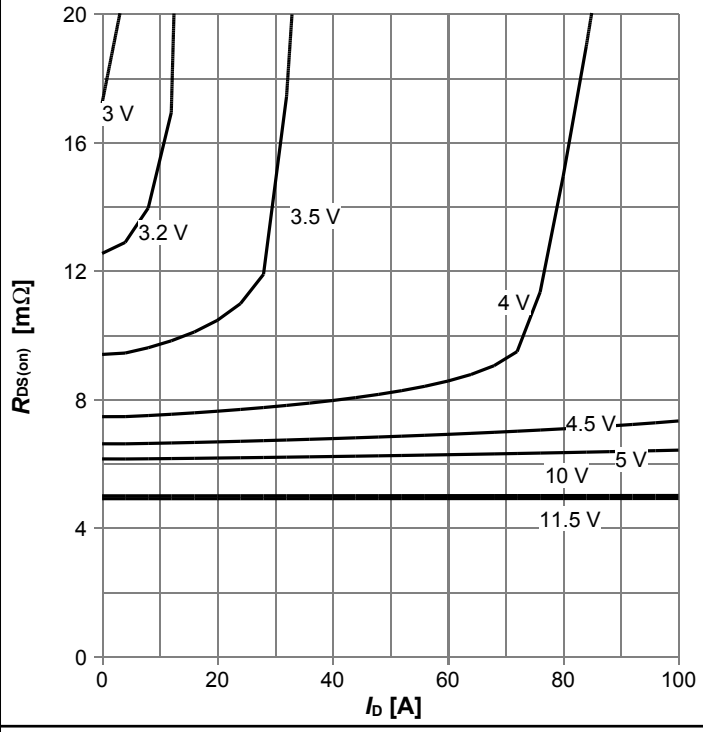
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



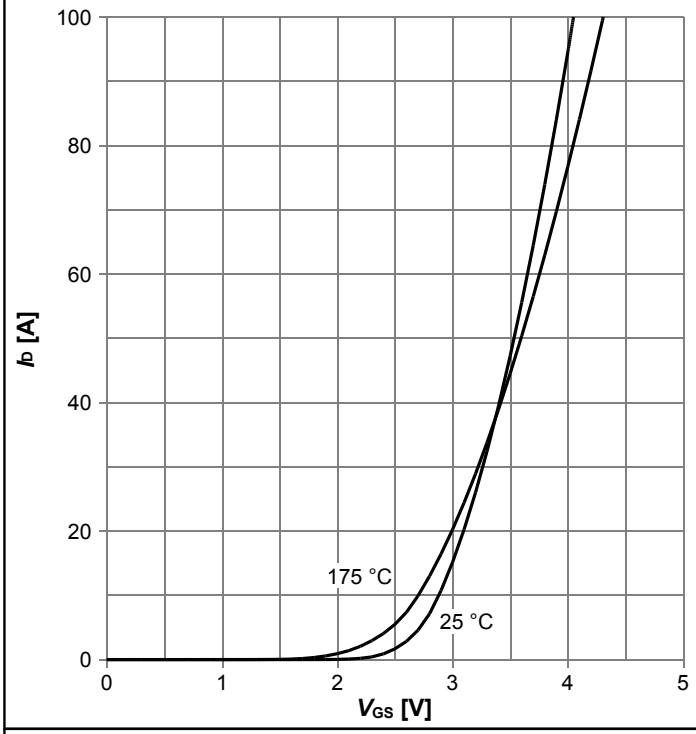
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



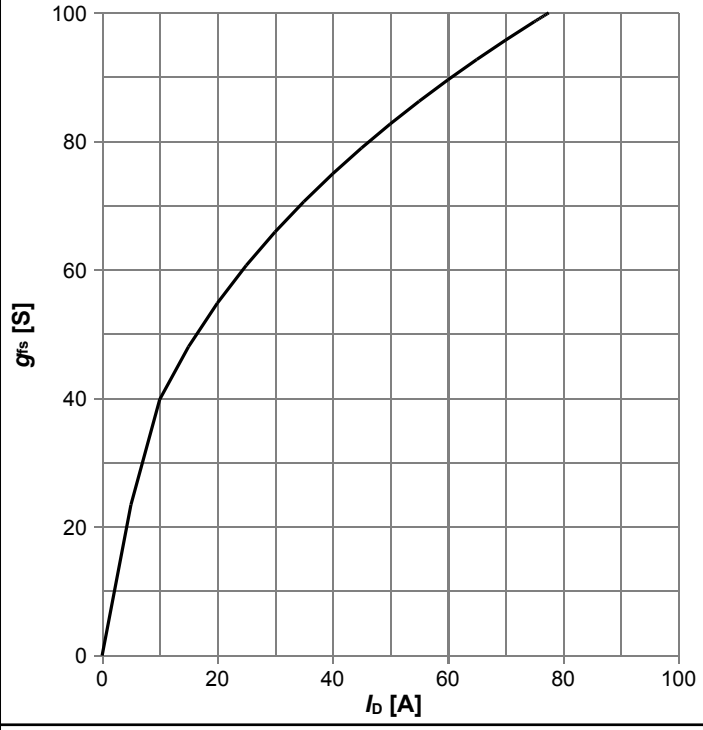
$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



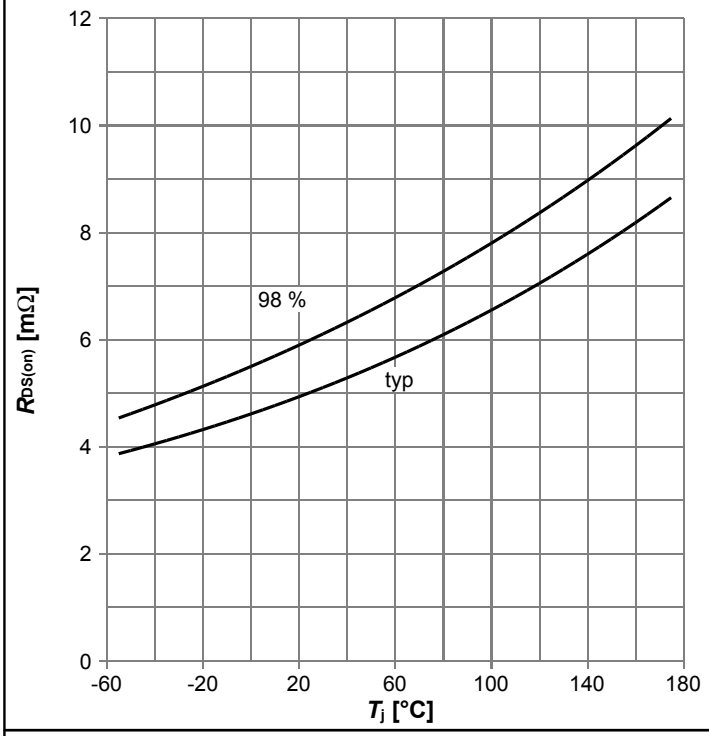
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



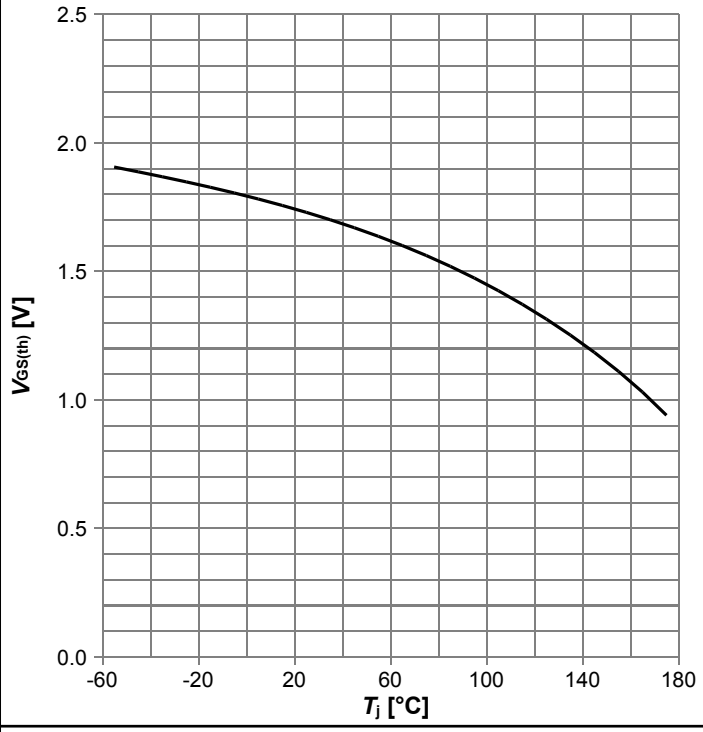
$g_{fs}=f(I_D)$; $T_j=25$ °C

Diagram 9: Drain-source on-state resistance



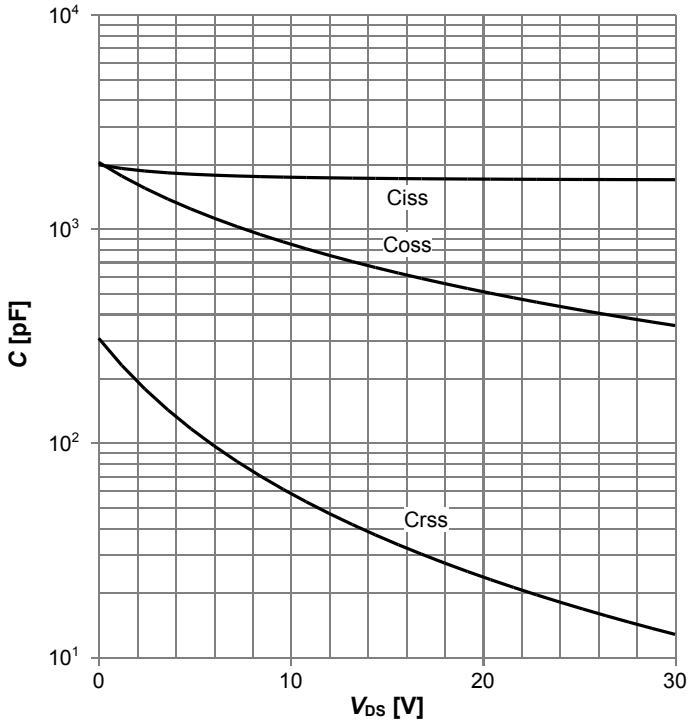
$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



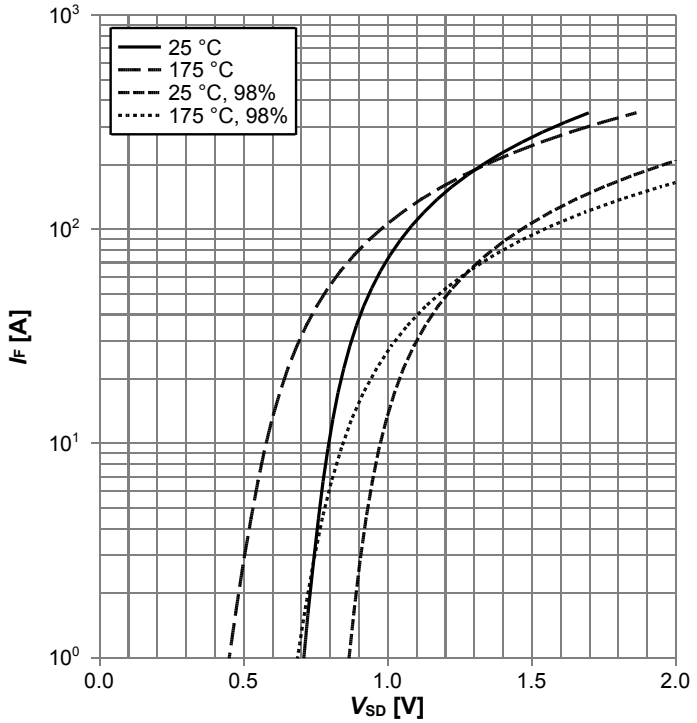
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA

Diagram 11: Typ. capacitances



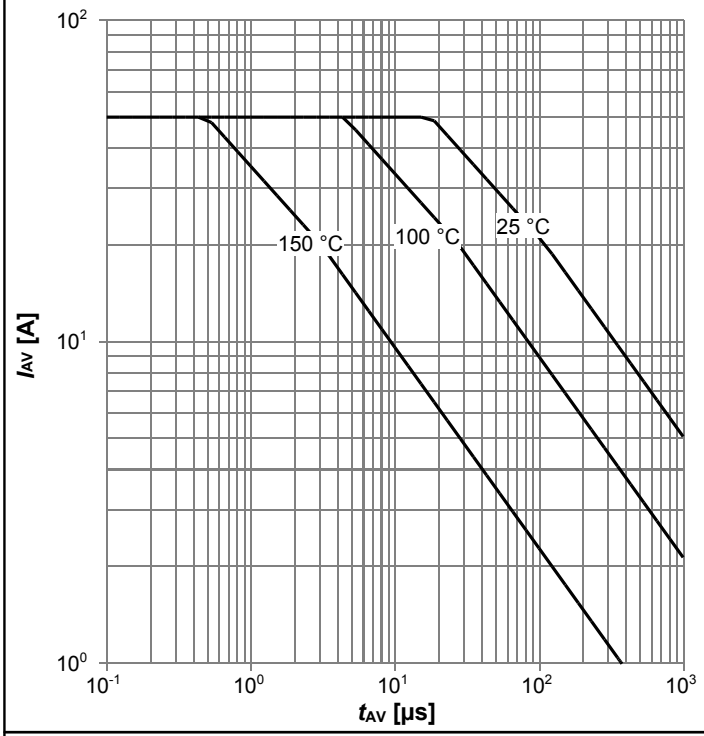
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



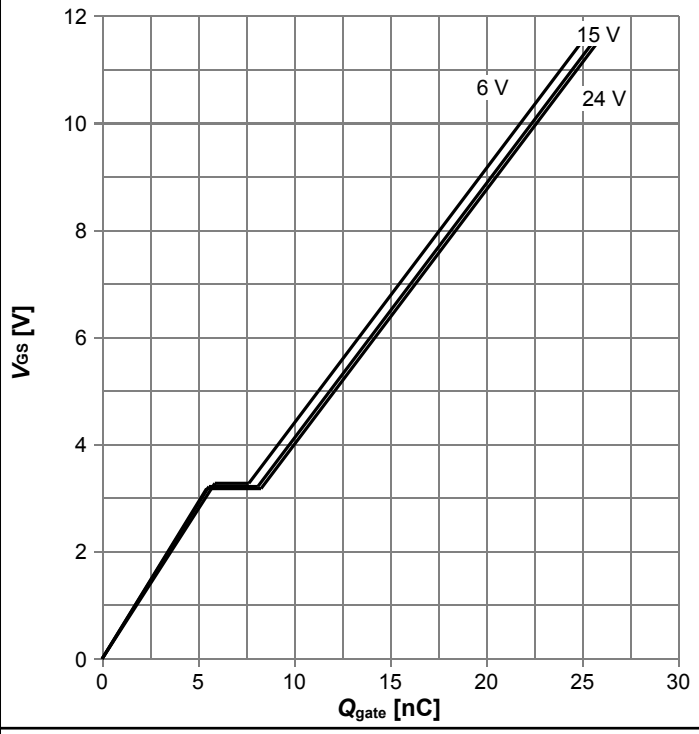
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



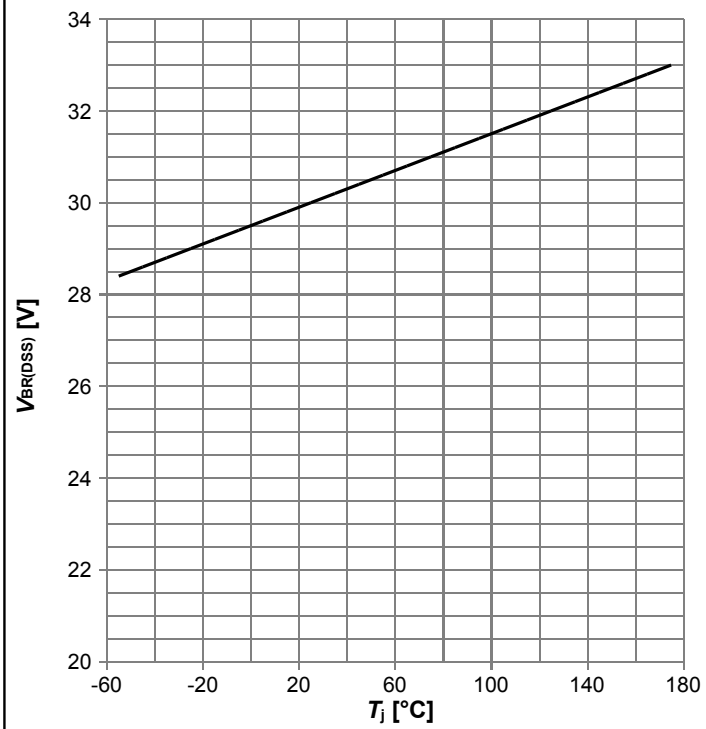
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



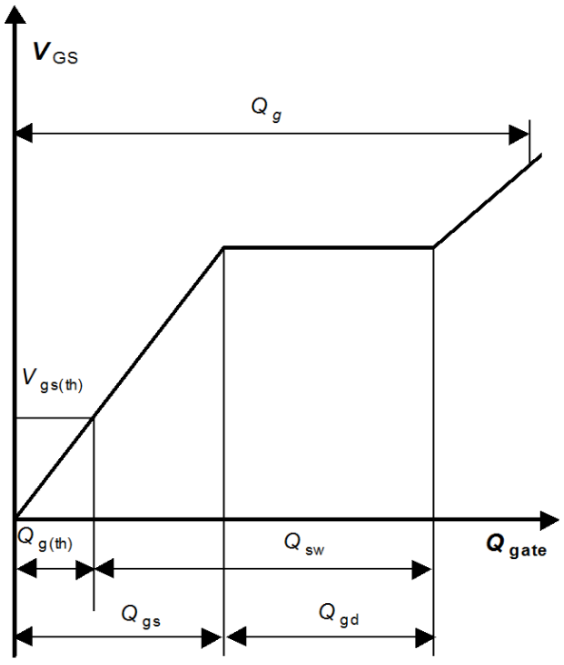
V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

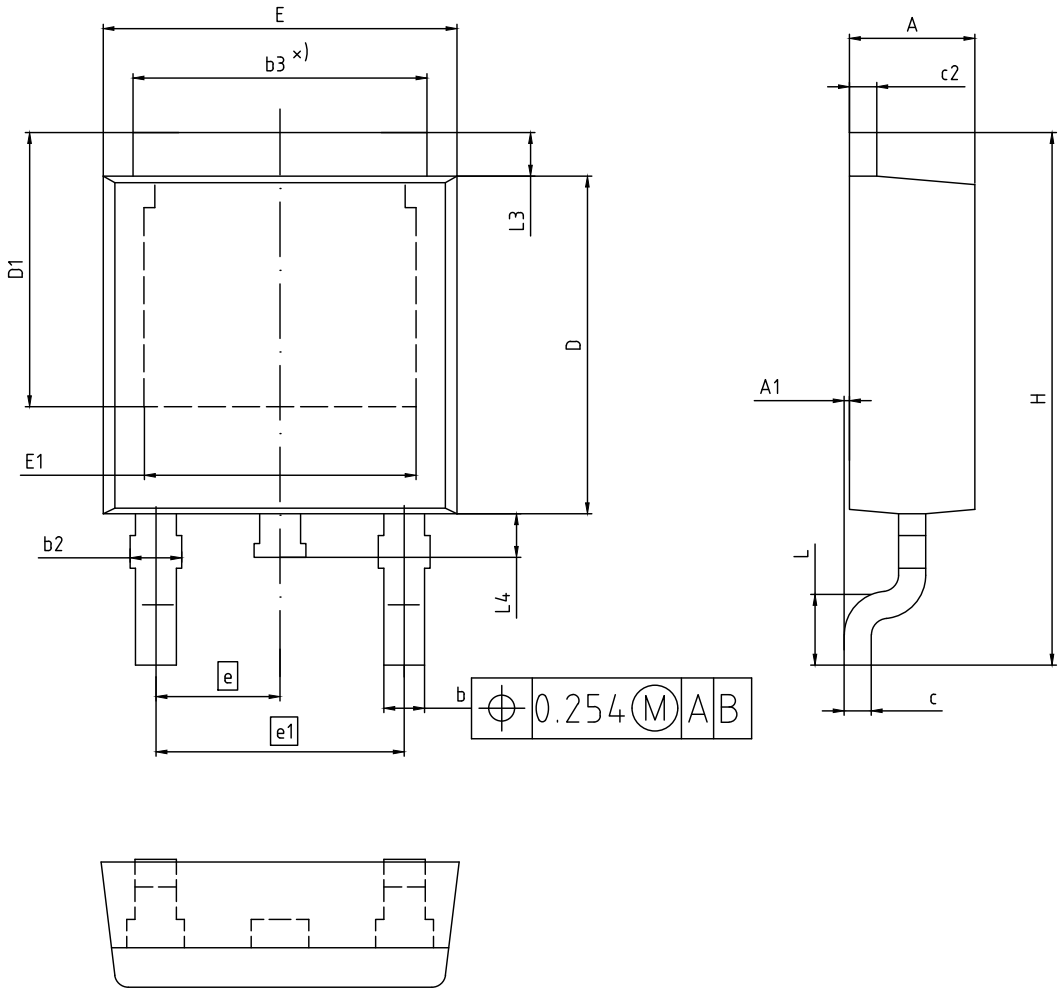


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



ALL DIMENSIONS REFER TO JEDEC
STANDARD TO-252 AND DO NOT INCLUDE MOLD
FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4.95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

DOCUMENT NO.	Z8B00003328
REVISION	07
SCALE:	10:1
	0 1 2mm
EUROPEAN PROJECTION	
ISSUE DATE	01.04.2020

Figure 1 Outline PG-TO252-3, dimensions in mm

Revision History

IPD060N03L G

Revision: 2020-09-14, Rev. 2.2

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.2	2020-09-14	Update POD

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