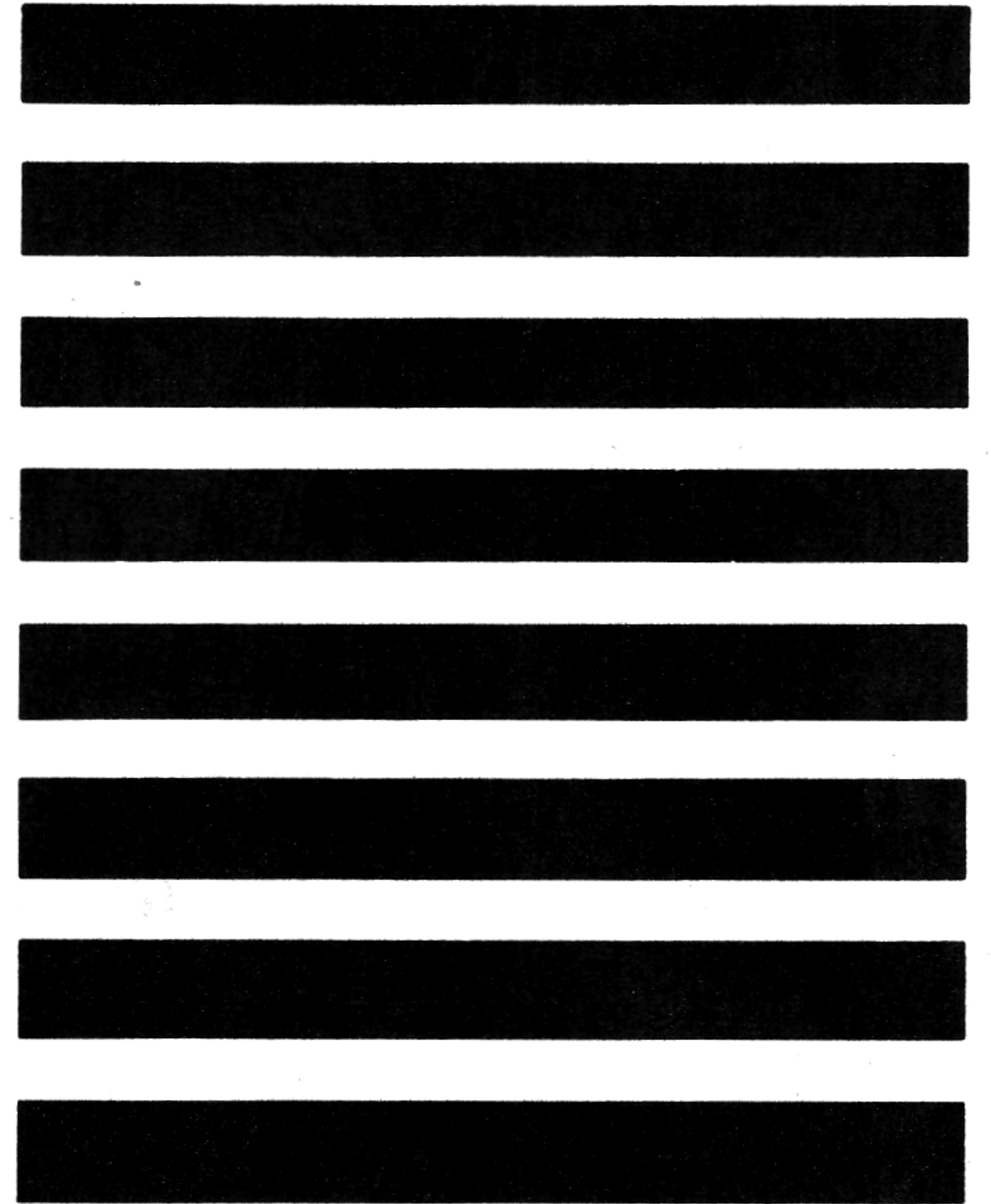




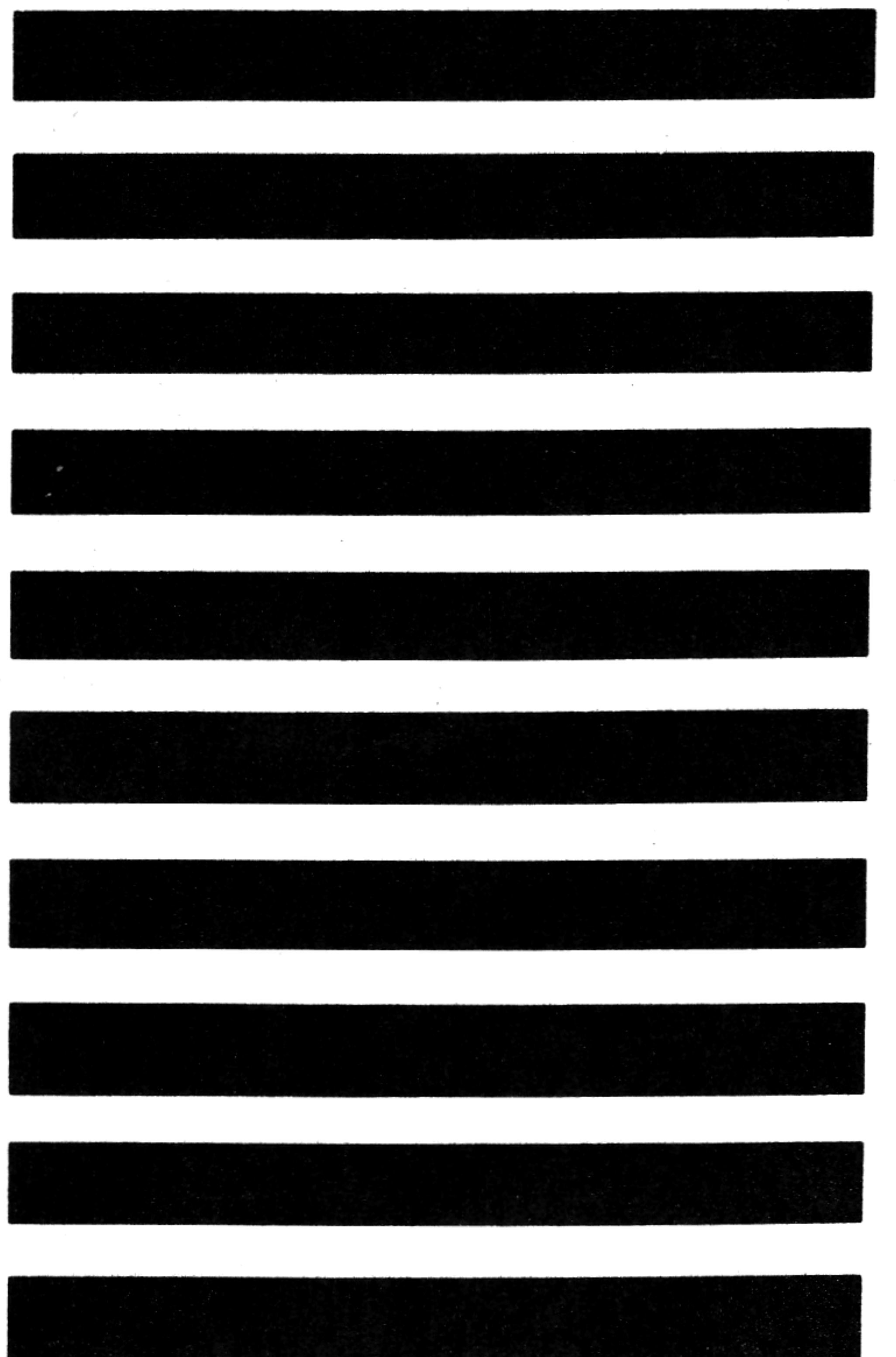
MOTOROLA

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MHTL

**INTEGRATED CIRCUITS
MC660 SERIES**





MHTL

MC660 SERIES INTEGRATED CIRCUITS

INDEX

Functions and Characteristics
General Information
Logic Diagram Summary of Devices Available

DEVICE SPECIFICATIONS

MC660	Expandable Dual 4-Input NAND Gate (active pullup)
MC661	Expandable Dual 4-Input NAND Gate (passive pullup)
MC662	Expandable Dual 4-Input Line Driver
MC663	Dual J-K Flip-Flop
MC664	Master-Slave R-S Flip-Flop
MC665	Triple Level Translator
MC666	Triple Level Translator
MC667	Dual Monostable Multivibrator
MC668	Quad 2-Input NAND Gate (passive pullup)
MC669	Dual 4-Input Expander
MC670	Triple 3-Input NAND Gate (passive pullup)
MC671	Triple 3-Input NAND Gate (active pullup)
MC672	Quad 2-Input NAND Gate (active pullup)
MC673	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate (active pullup)
MC674	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate (passive pullup)

FUNCTIONS AND CHARACTERISTICS

($V_{CC} = 15 \text{ Vdc}$ $T_A = 25^\circ\text{C}$)

Function	Type Case 605, 632 -30 to +75°C	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation mW Typ/pkg
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GATES

Expandable Dual 4-Input NAND Gate (active pullup)	MC660	10	110	88/26 ①
Expandable Dual 4-Input NAND Gate (passive pullup)	MC661	10	125	88/26 ①
Quad 2-Input NAND Gate (passive pullup)	MC668	10	125	176/52 ①
Triple 3-Input NAND Gate (passive pullup)	MC670	10	125	132/39 ①
Triple 3-Input NAND Gate (active pullup)	MC671	10	110	132/39 ①
Quad 2-input NAND Gate (active pullup)	MC672	10	110	176/52 ①
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate (active pullup)	MC673	10	110	160/50 ①
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate (passive pullup)	MC674	10	125	160/50 ①

DRIVER

Expandable Dual 4-Input Line Driver	MC662	10	140	180/26 ①
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FLIP-FLOPS

Dual J-K Flip-Flop	MC663	10	3.0 MHz ②	200
Master-Slave R-S Flip-Flop	MC664	10	3.0 MHz ②	160

EXPANDER

Dual 4-Input Expander	MC669	—	—	—
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MULTIVIBRATOR

Dual Monostable Multivibrator	MC667	10	—	240
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TRANSLATORS

Triple Level Translator	MC665	MDTL = 8 MTTL III = 5.5 MRTL = 5	30	83 (DTL) 104 (RTL)
Triple Level Translator	MC666	10	75	105

L suffix denotes Ceramic Package, P suffix denotes Plastic Package.

① Inputs High/Input Low

② f_{Tog}

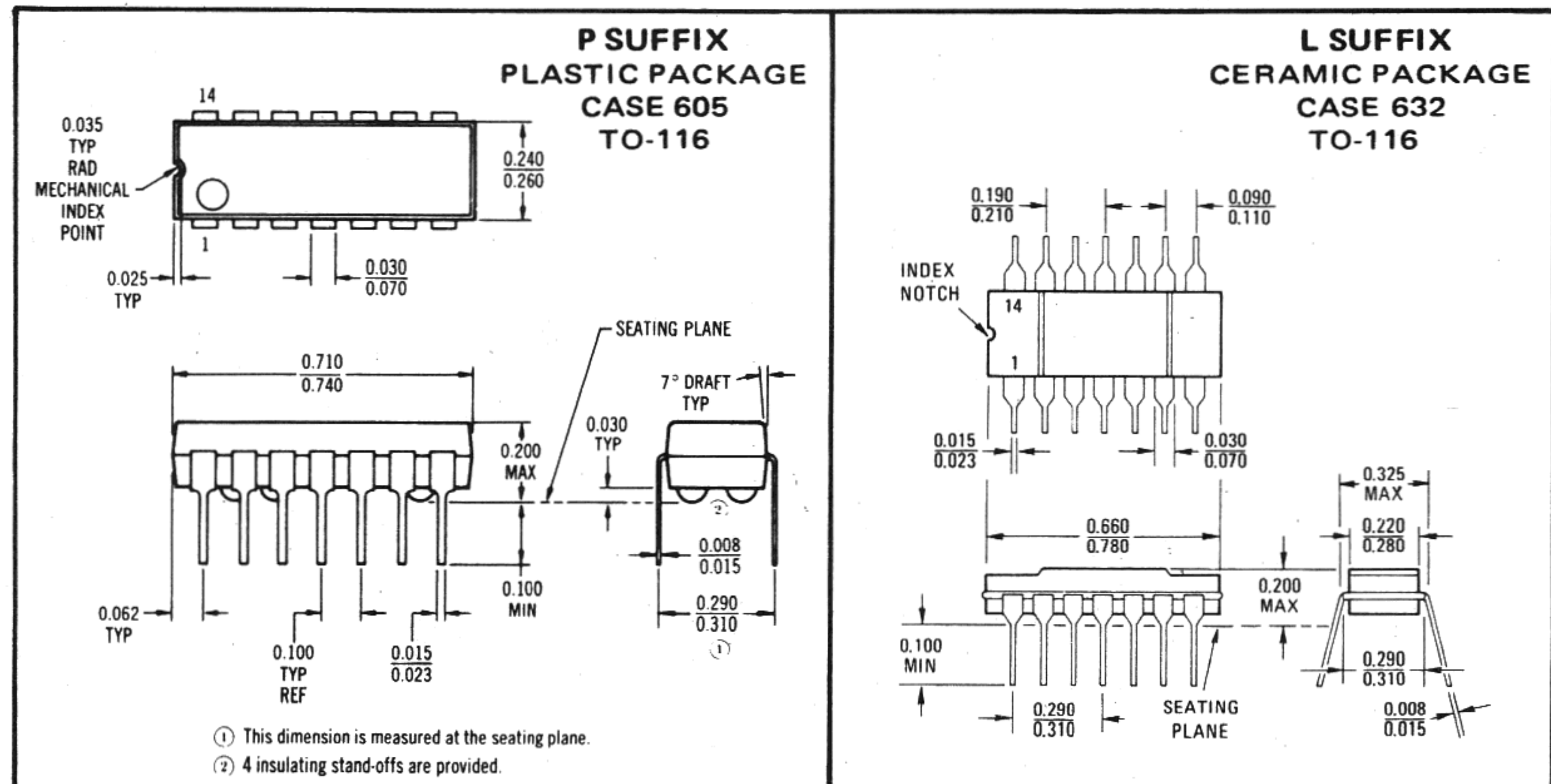
GENERAL INFORMATION

MHTL MC660 series

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PACKAGING

All MHTL integrated circuits are available in the TO-116 14-lead dual in-line ceramic package (add suffix L to type number when ordering) and in the TO-116, 14-lead dual in-line plastic package (suffix P).



MAXIMUM RATINGS $T_A = 25^\circ\text{C}$

Rating	Symbol	Value	Unit
Power Supply Voltage Continuous Pulsed, 1.0 s	V_{CC}	18 20	Vdc
Input Voltage MC666 DTL RTL All Others	V_{in}	-1.0 to +6.0 -4.0 to +4.0 -1.0 to +18	Vdc
Output Current (into outputs) MC662 MC663 MC664 MC669 All Others	—	60 28 26 — 30	mAdc
Input Reverse Current @ 18 V	I_R	0.5	mAdc
Forward Current (Individual) MC669P	I_F	30	mAdc
Operating Temperature Range	T_A	-30 to +75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$

TEST LIMITS TOLERANCE

$$T_A = \pm 3^\circ\text{C} \quad V_R = \pm 1\% \quad V_{CC} = \pm 1\% \quad V_{IL} = \pm 1\% \quad V_{IH} = \pm 1\% \quad V_F = \pm 1\% \quad I_{OL} = \pm 1\% \quad I_{OH} = \pm 1\%$$

DEFINITIONS

CP	Clock Pulse
I_{CEX}	Collector-to-emitter leakage of the output transistor
I_{CCH}	V_{CC} current drain when all inputs are high
I_{CCL}	V_{CC} current drain when all inputs are low
I_F	Forward current of input diodes for unit input load
$2I_F$	Forward current of input diodes which are equal to twice unit load
I_{OH}	Test current flowing into the output pin when output is high. (Negative)
I_{OL}	Test current flowing into output pin when output is low
I_R	Reverse current of input diodes with V_R applied
$2I_R$	Reverse current of two input diodes with V_R applied
I_{SC}	Short-circuit current obtained from device output when output is high

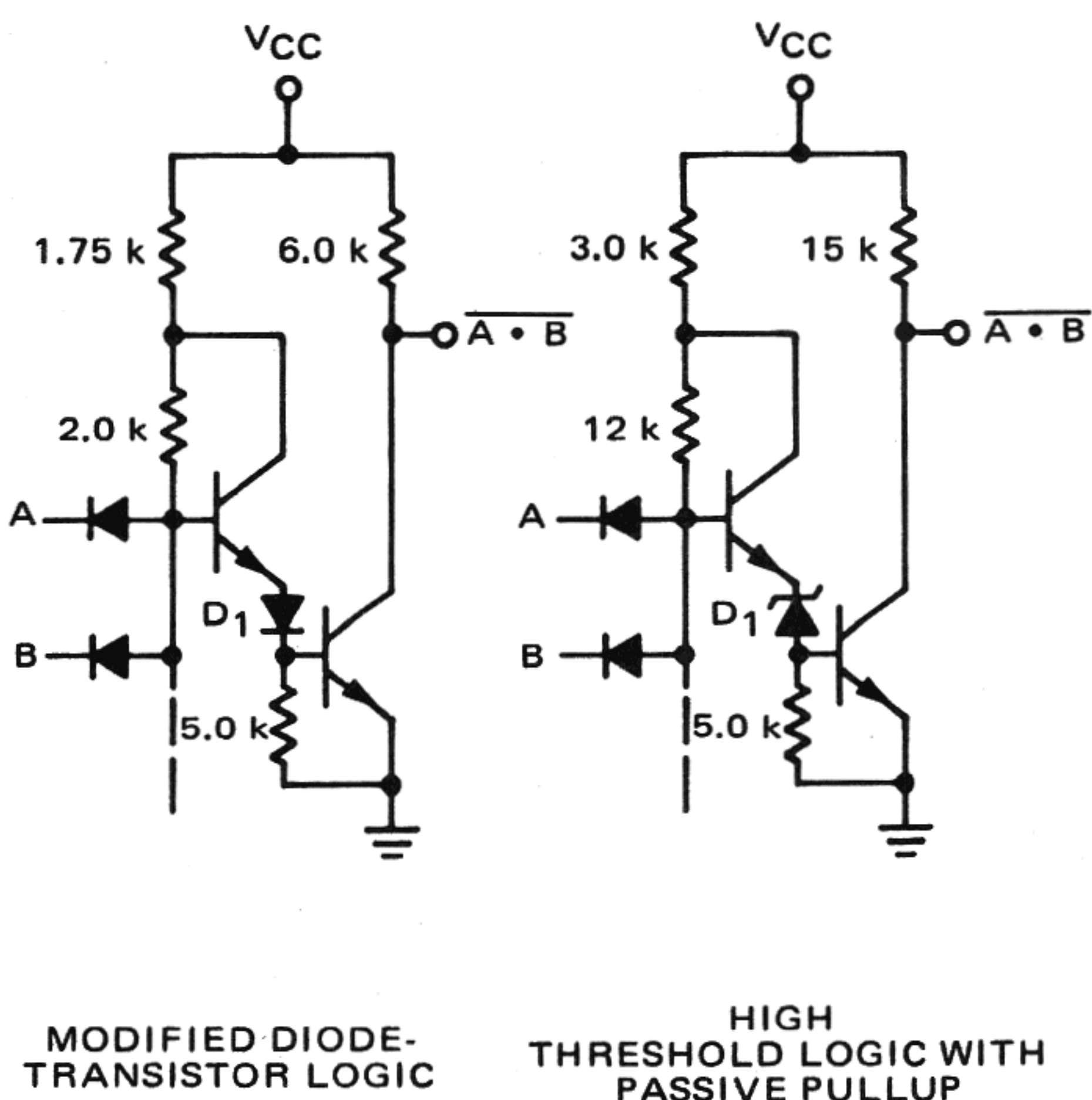
t_{pd+}	Propagation delay time for a positive-going output pulse
t_{pd-}	Propagation delay time for a negative-going output pulse
V_{CC}	Device power supply voltage
V_{CCH}	High power supply voltage
V_{CCL}	Low power supply voltage
V_{CEX}	Collector-to-emitter voltage of the output transistor
V_F	Input voltage when measuring I_F
V_{IH}	Threshold voltage for high input voltage state
V_{IL}	Threshold voltage for low input voltage state
V_{OH}	Output high voltage state with I_{OH} flowing out of pin
V_{OL}	Output low voltage state with I_{OL} flowing into pin
V_R	Reverse voltage for input diode leakage test
V_X	Threshold voltage for low input voltage state on expander unit

GENERAL RULES

- The number of load circuits that may be driven from an output is determined by the input loading factor. The summation of input loading should not exceed the drive capability of the output.
- The outputs of the passive pullup gates may be tied together to perform the wired-collector OR function. For each added gate subtract 1.2 output loading factor (fan-out).
- The outputs of the active pullup devices should not be tied together.

GENERAL INFORMATION (continued)

FIGURE 1—GATE COMPARISONS



HIGH THRESHOLD LOGIC

The High Threshold Logic (MHTL) family of integrated circuit devices was developed for applications requiring a higher degree of inherent electrical noise immunity than is available with the more standard forms of integrated circuit logic families. The basic MHTL logic gate is similar to the Diode Transistor Logic (MDTL) gate circuit as can be seen in Figure 1. A considerably larger input threshold characteristic is exhibited by the MHTL devices by using a reversed biased base-emitter junction which operates in the breakdown avalanche mode (sometimes referred to as zener operation) as compared to a forward biased diode junction for the corresponding D_1 element in the MDTL gate. A typical 7.5 volt input signal is required to turn on the MHTL output inverting transistor while a 1.5 volt signal is necessary for MDTL.

The higher threshold characteristic of MHTL requires a higher V_{CC} supply and is specified at 15 volts ± 1.0 V tolerance. In order to keep the power dissipation within reasonable levels, higher values of resistance are used in MHTL than for corresponding resistors in the MDTL circuit. These resistance values also allow the outputs of gates to be interconnected to provide the "wired-OR" logic function. The propagation delay of MHTL is in the order of 110 nanoseconds and consequently is a relatively slow logic family, a property which aids in rejecting noise. A comparison of transfer curves is made in Figure 2 illustrating the large logic swing available from MHTL.

An active output pullup configuration is available for the MHTL devices and is shown in Figure 3. The active output arrangement will allow the circuits to handle capacitive loads at a higher speed than is obtainable with the passive pullup configuration. Additionally, the impedance in the high state is considerably less, and consequently makes the family more immune to electrical noise. The active output configuration also allows for a more powerful arrangement to interface with discrete components.

In summary the MHTL devices may be characterized as an integrated circuit family with a high degree of inherent noise immunity, a high input threshold and a large logic swing. These characteristics make the line very attractive for use where electrical noise is an important consideration, as well as for applications where interfacing with various discrete components is required.

FIGURE 2—TRANSFER CURVES

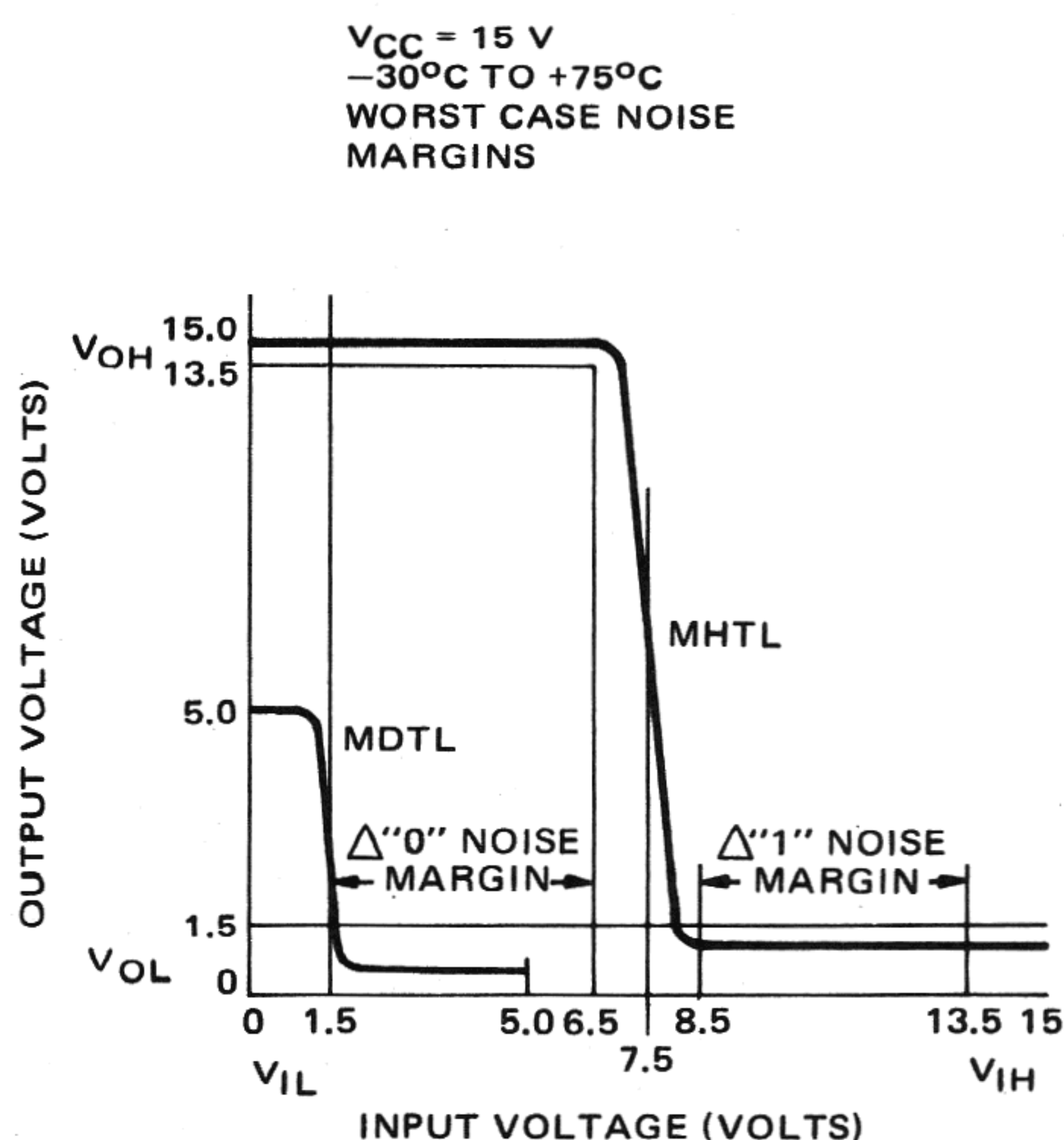
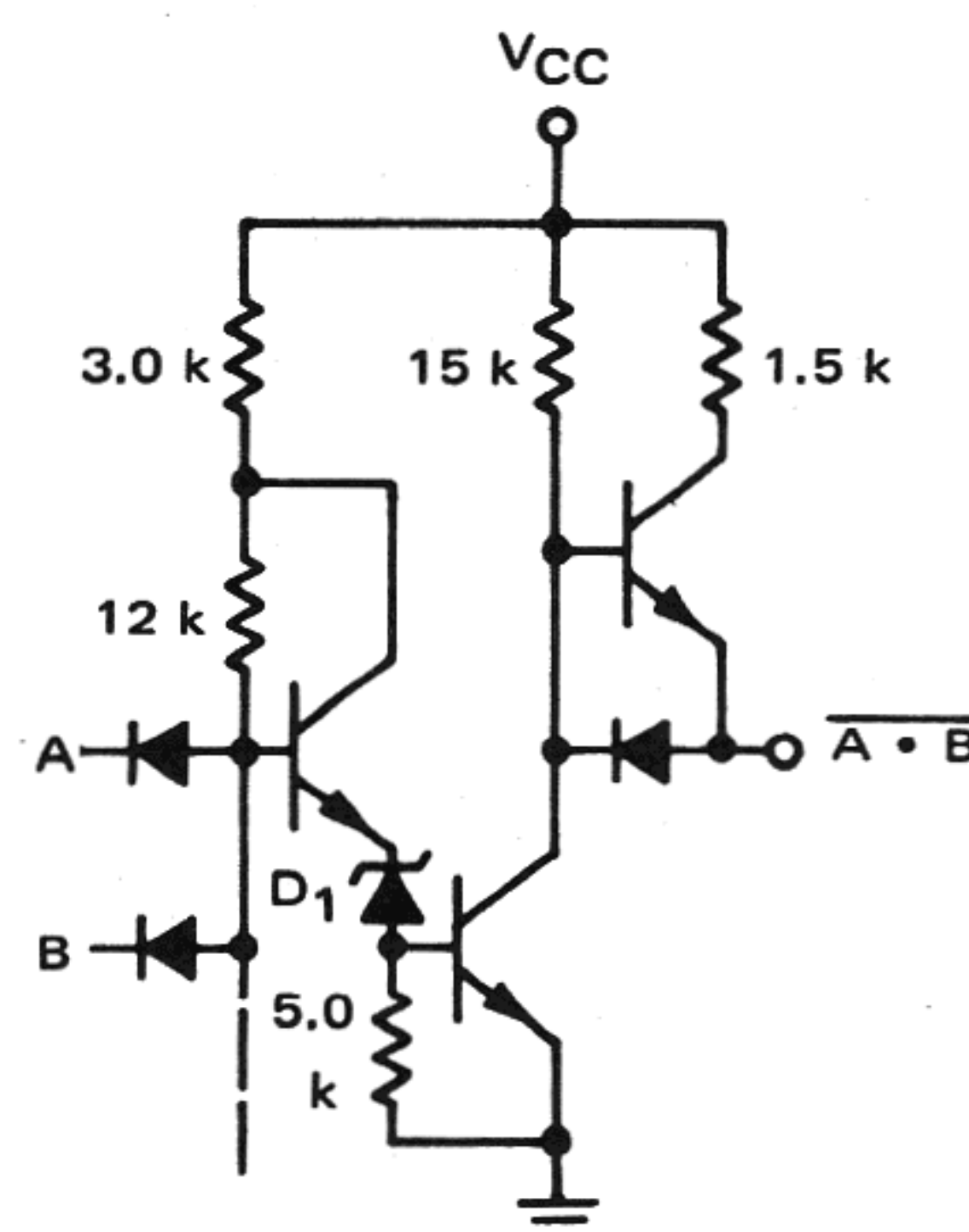


FIGURE 3—MHTL GATE WITH ACTIVE PULLUP



LOGIC DIAGRAMS

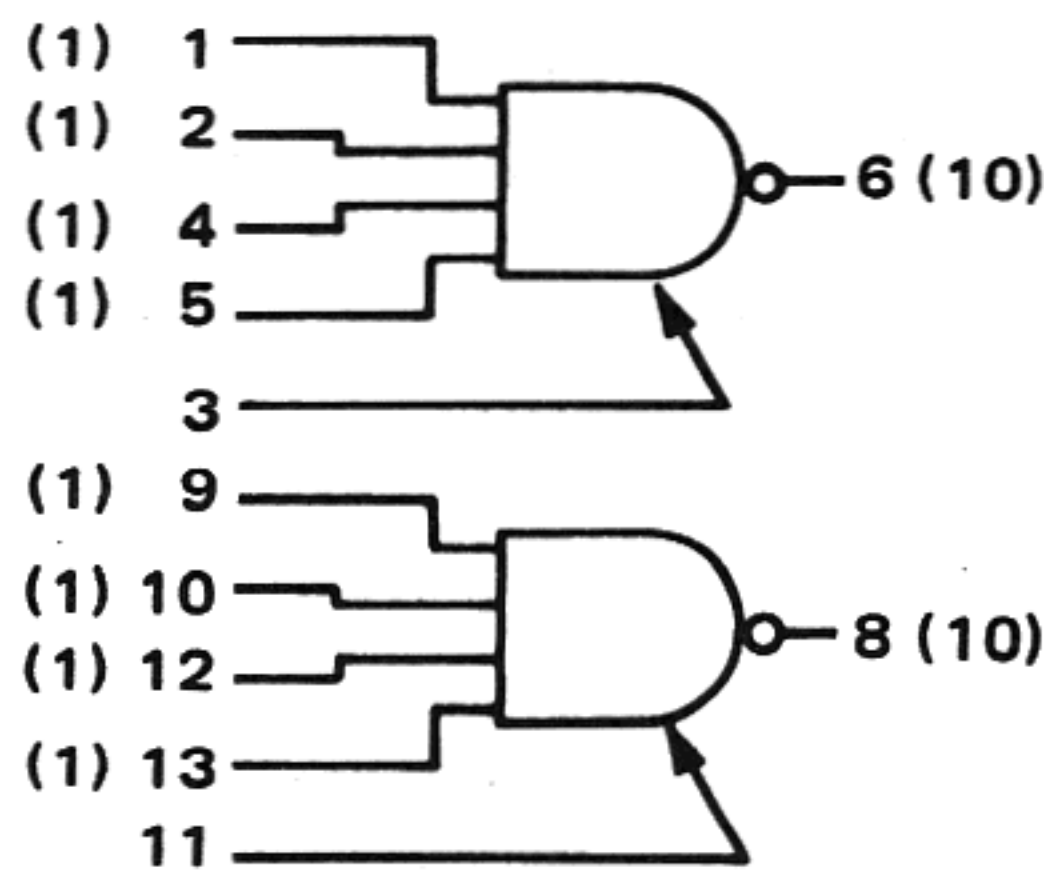
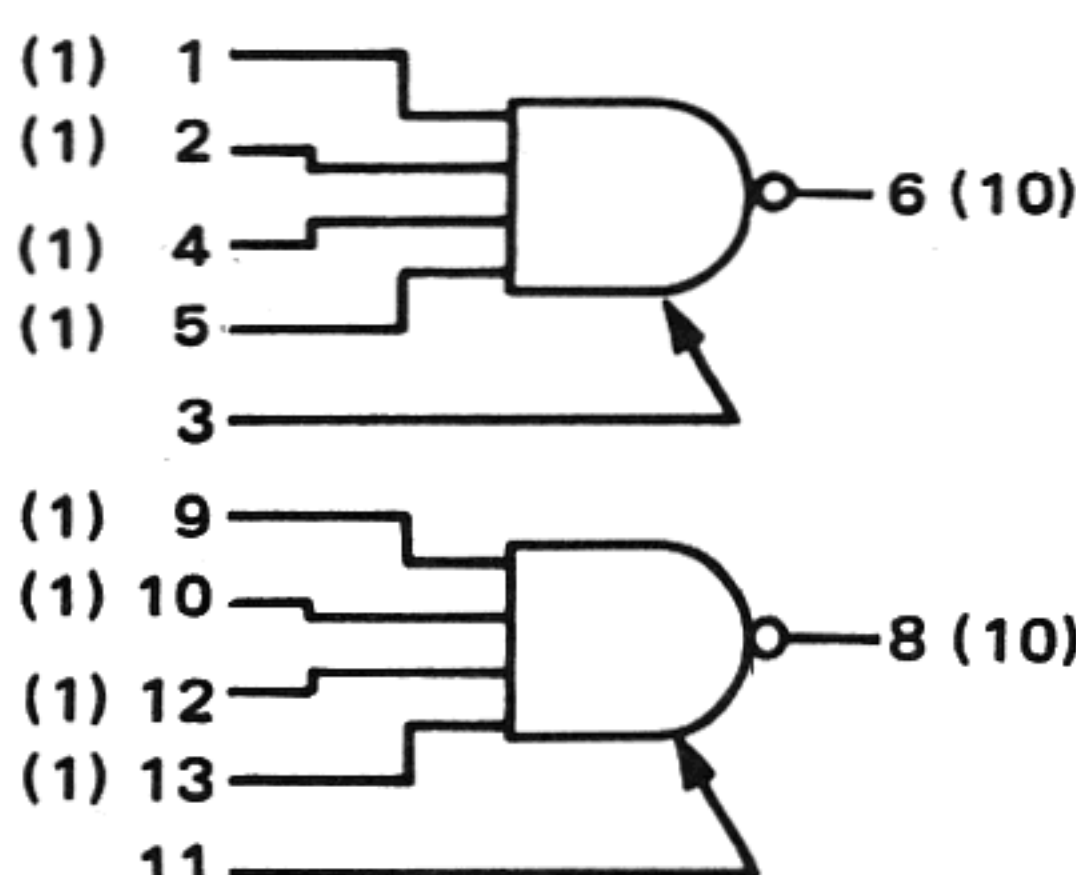
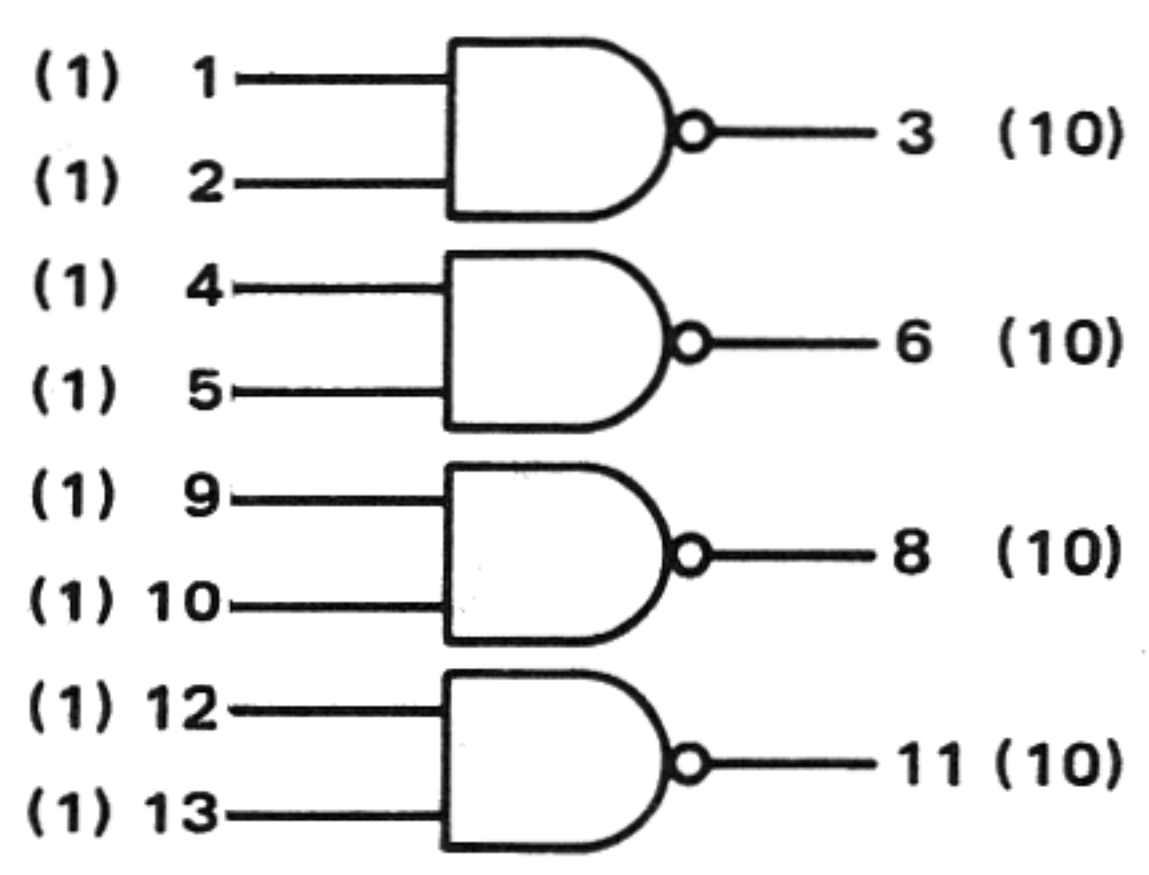
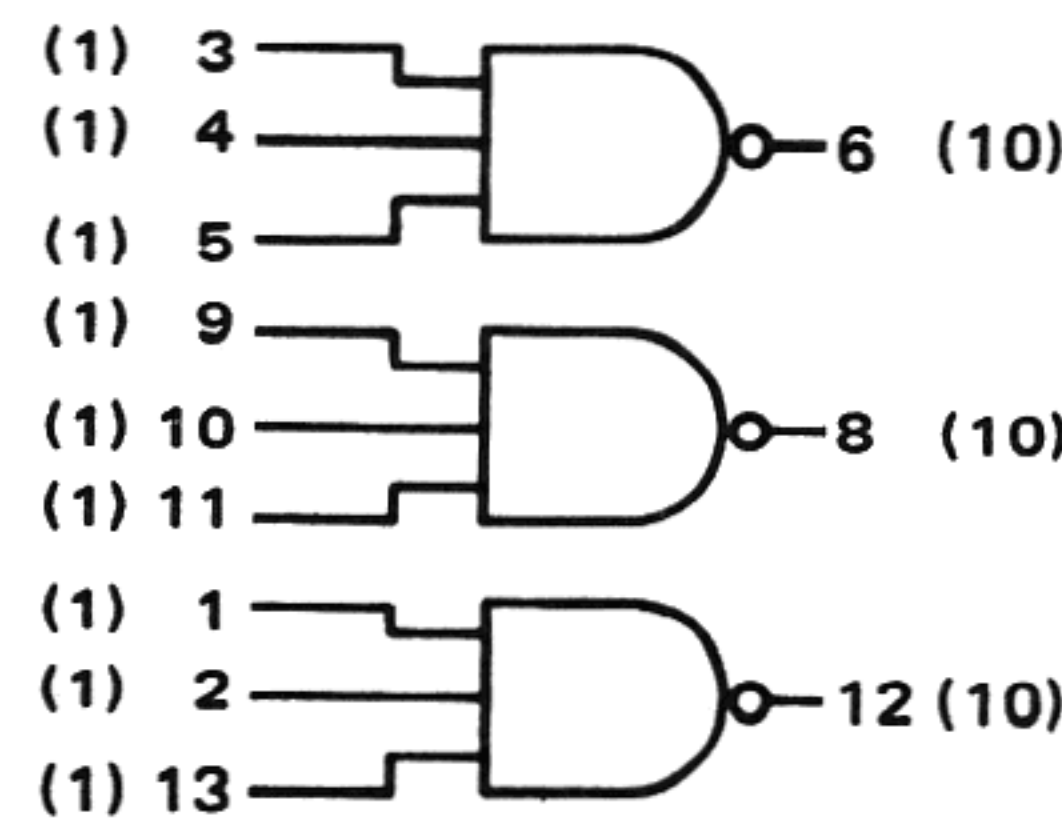
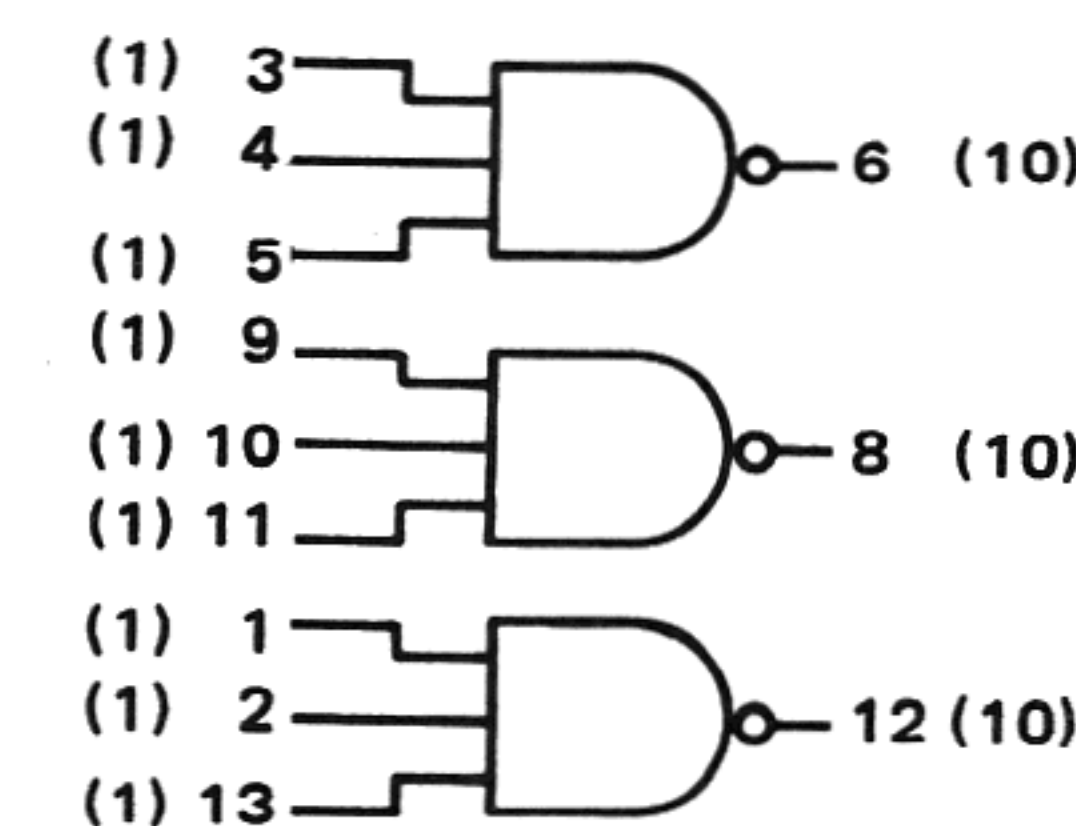
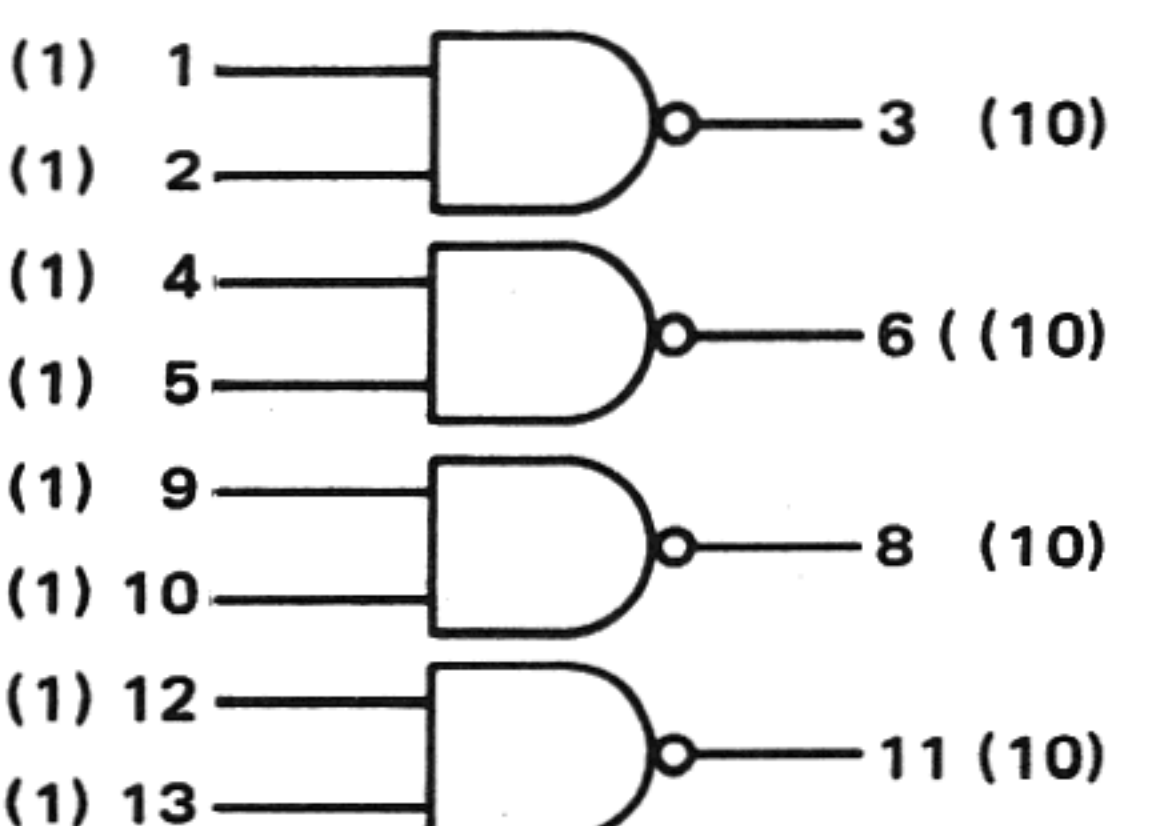
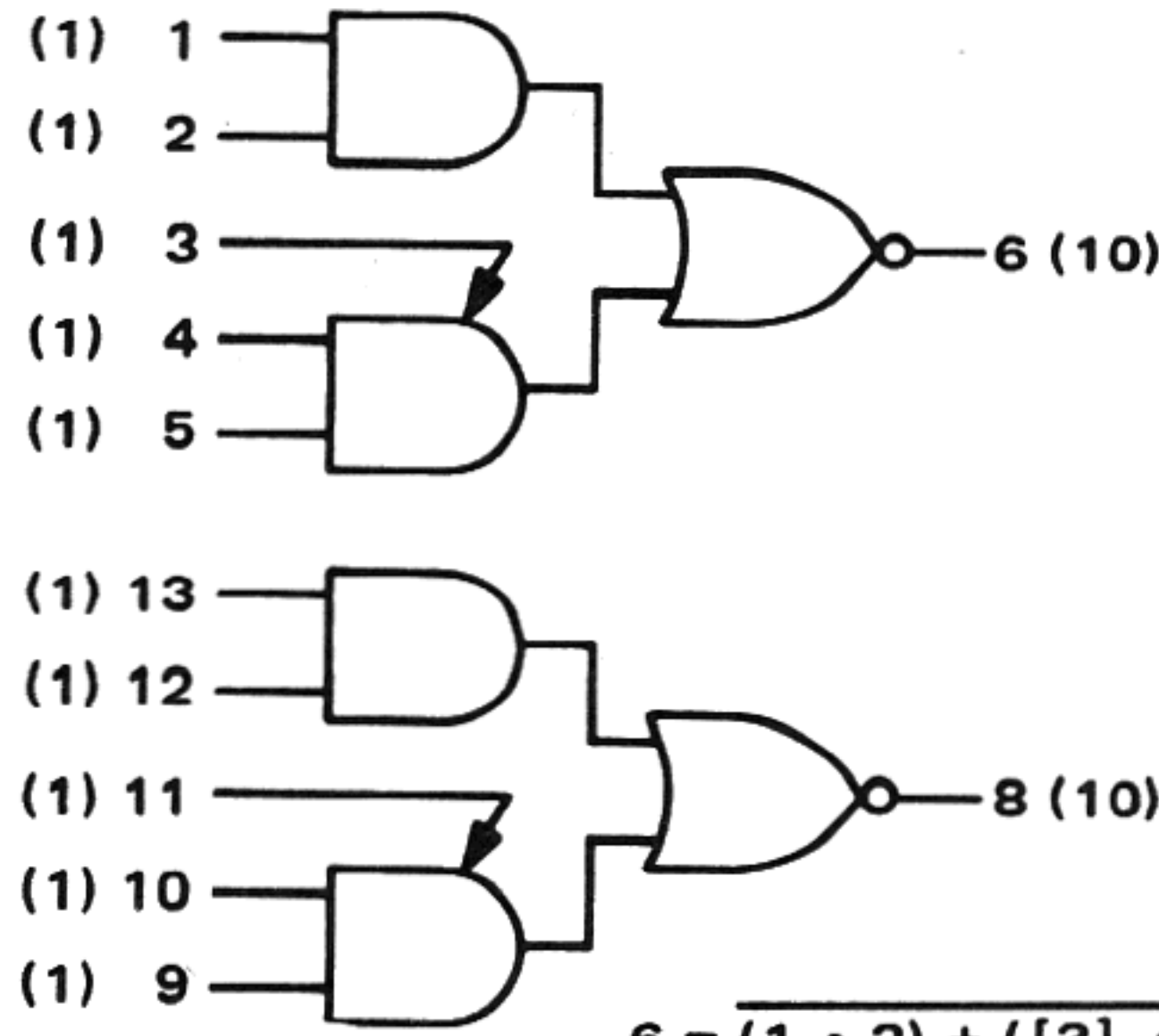
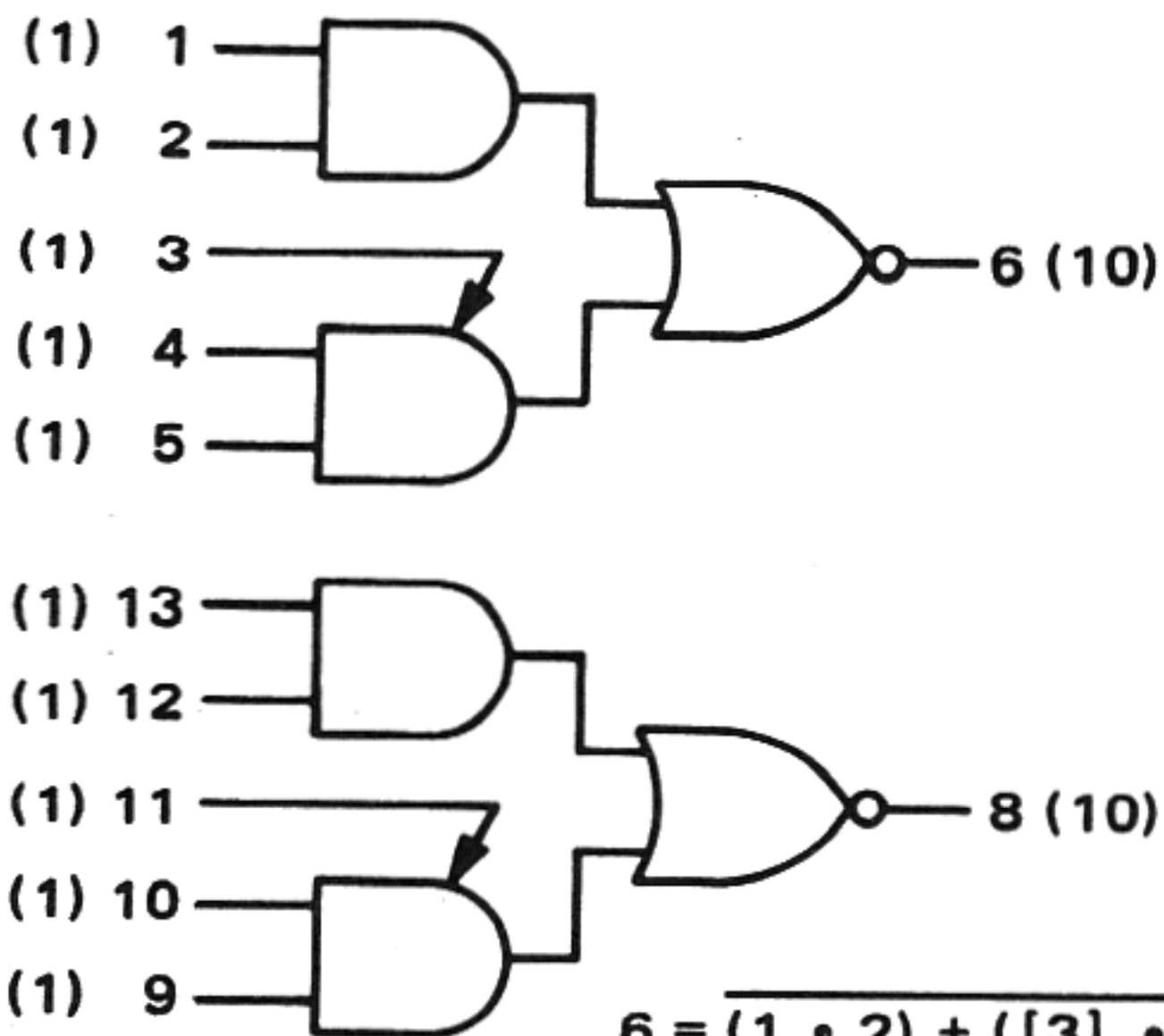
MHTL MC660 series

The logic diagrams shown describe the circuits of the MHTL line and permit quick selection of circuits required to implement a particular logic system. Pertinent information, such as logic equations and truth tables is provided to show line compatibility. Package pin numbers and loading factors for each device are specified with each logic diagram. The numbers at the ends of the terminals are package pin numbers. Numbers in parenthesis indicate loading.

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(V_{CC} = Pin 14, Gnd = Pin 7)

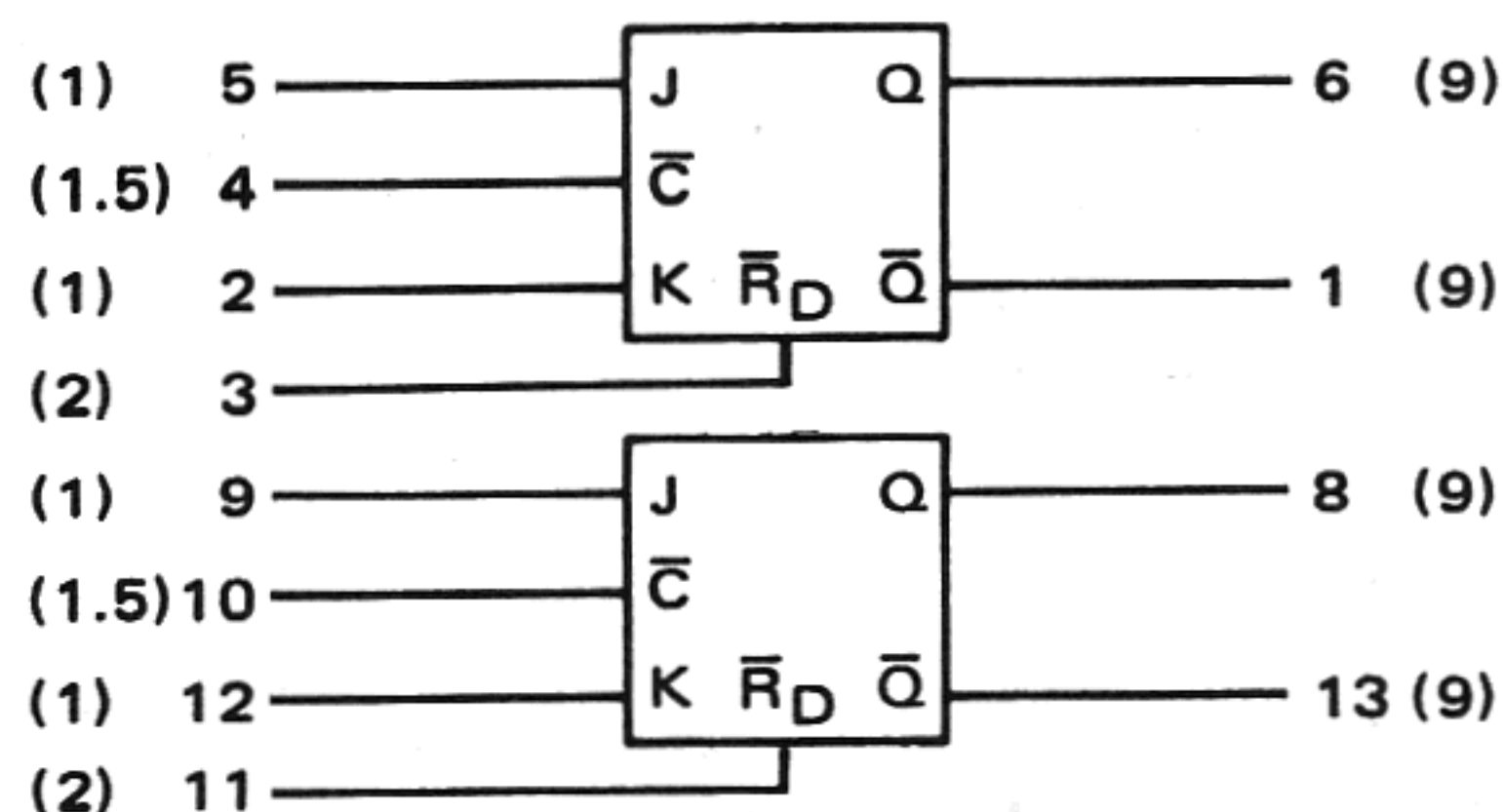
GATES

MC660 Expandable Dual 4-Input NAND Gate (active output pullup)  $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$ t_{pd} = 110 ns typ P_D = 88 mW typ/pkg (Inputs High) 26 mW typ/pkg (Input Low)	MC661 Expandable Dual 4-Input NAND Gate (passive output pullup)  $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$ t_{pd} = 125 ns typ P_D = 88 mW typ/pkg (Inputs High) 26 mW typ/pkg (Input Low)	MC668 Quad 2-Input NAND Gate (passive output pullup)  $3 = \overline{1 \cdot 2}$ t_{pd} = 125 ns typ P_D = 176 mW typ/pkg (Inputs High) 52 mW typ/pkg (Input Low)
MC670 Triple 3-Input NAND Gate (passive output pullup)  $6 = \overline{3 \cdot 4 \cdot 5}$ t_{pd} = 125 ns typ P_D = 132 mW typ/pkg (Inputs High) 39 mW typ/pkg (Input Low)	MC671 Triple 3-Input NAND Gate (active output pullup)  $6 = \overline{3 \cdot 4 \cdot 5}$ t_{pd} = 110 ns typ P_D = 132 mW typ/pkg (Inputs High) 39 mW typ/pkg (Input Low)	MC672 Quad 2-Input NAND Gate (active output pullup)  $3 = \overline{1 \cdot 2}$ t_{pd} = 110 ns typ P_D = 176 mW typ/pkg (Inputs High) 52 mW typ/pkg (Input Low)
MC673 Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate (active output pullup)  $6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$ t_{pd} = 110 ns typ P_D = 160 mW typ/pkg (Inputs High) 50 mW typ/pkg (Input Low)	MC674 Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate (passive output pullup)  $6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$ t_{pd} = 125 ns typ P_D = 160 mW typ/pkg (Inputs High) 50 mW typ/pkg (Input Low)	

LOGIC DIAGRAMS (continued)

FLIP-FLOPS

MC663
Dual J-K Flip-Flop



$f_{Tog} = 3.0 \text{ MHz typ}$
 $P_D = 200 \text{ mW typ/pkg}$

TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\bar{Q}_n$	Q_n

Direct input ($\bar{R}_D$) must be high.

0 = low state

1 = high state

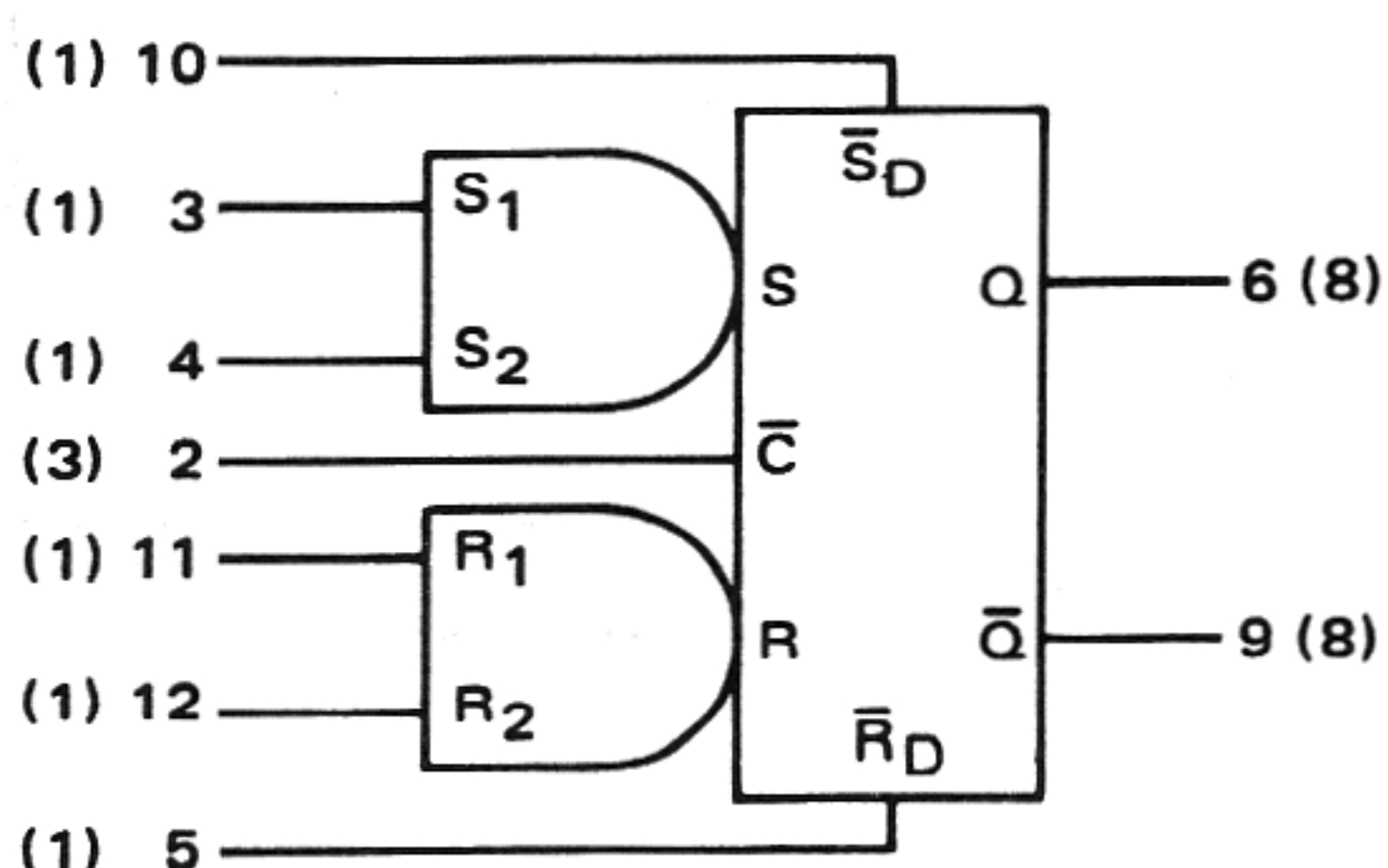
t_n = time period prior to negative transition of clock pulse

t_{n+1} = time period subsequent to negative transition of clock pulse

Q_n = state of Q output in time period t_n

NOTE: A low state "0" at the direct reset $\bar{R}_D$ causes a low state "0" at the Q output and the complement at the $\bar{Q}$ output.

MC664
Master-Slave R-S Flip-Flop



$f_{Tog} = 3.0 \text{ MHz typ}$
 $P_D = 160 \text{ mW typ/pkg}$

DIRECT INPUT OPERATION

$\bar{R}_D$	$\bar{S}_D$	Q	$\bar{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

Clock Input ($\bar{C}$) must be low

0 = low state

1 = high state

NC = No change

NA = Not allowed

X = state of input does not affect state of the circuit

U = indeterminate state

t_n = time period prior to negative transition of clock pulse

t_{n+1} = time period subsequent to negative transition of clock pulse

Q_n = state of Q output in time period t_n

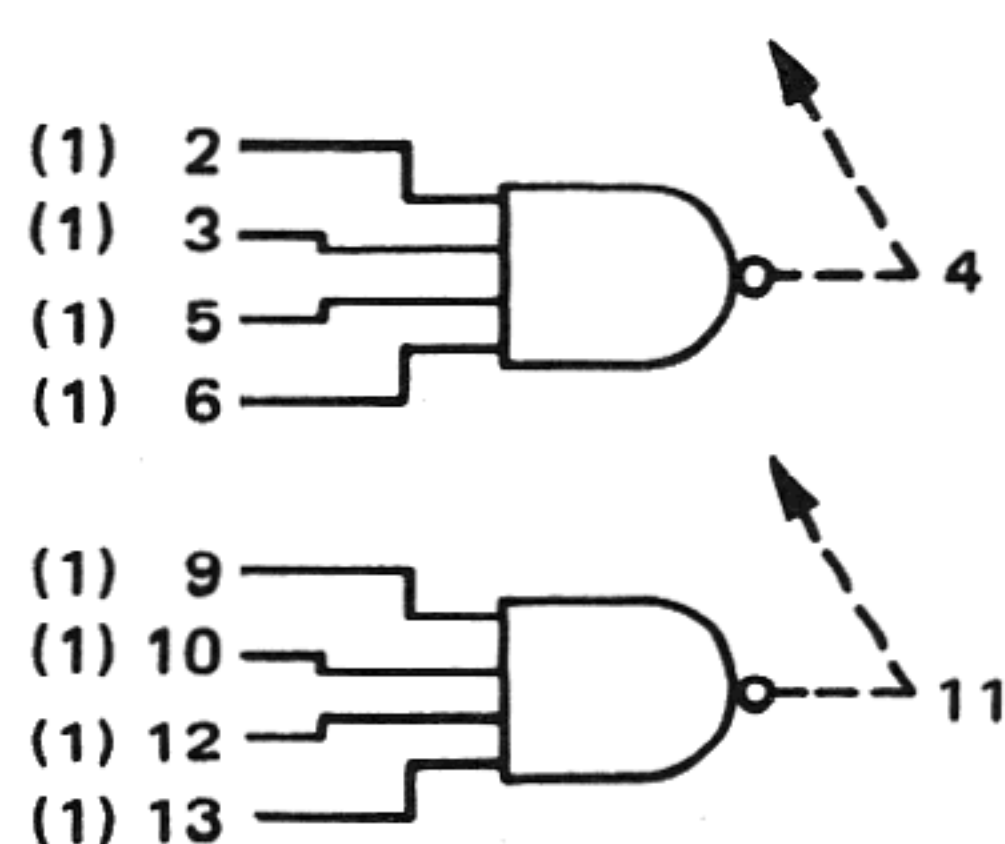
CLOCKED OPERATION

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

Direct inputs ($\bar{R}_D$, $\bar{S}_D$) must be high.

EXPANDER

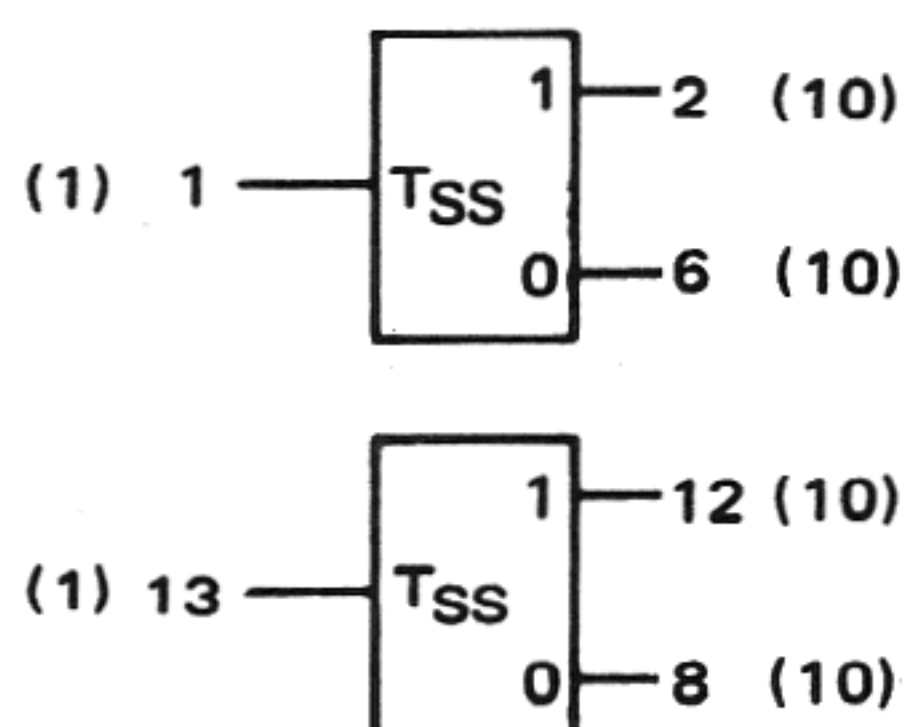
MC669
Dual 4-Input Expander



$$4 = 2 \cdot 3 \cdot 5 \cdot 6$$

MULTIVIBRATOR

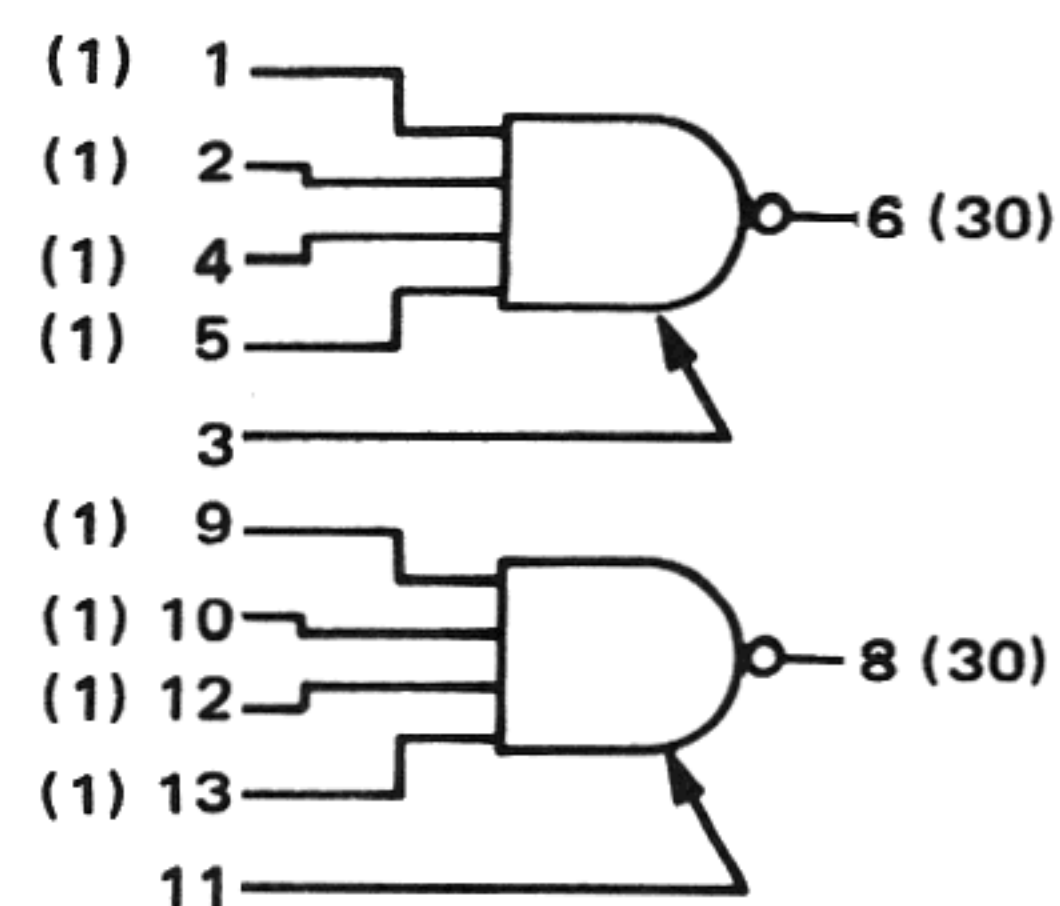
MC667
Dual Monostable Multivibrator



$t_{pd} = 140 \text{ ns typ}$
 $P_D = 240 \text{ mW typ/pkg}$

DRIVER

MC662
Expandable
Dual 4-Input Line Driver
(active output pullup)



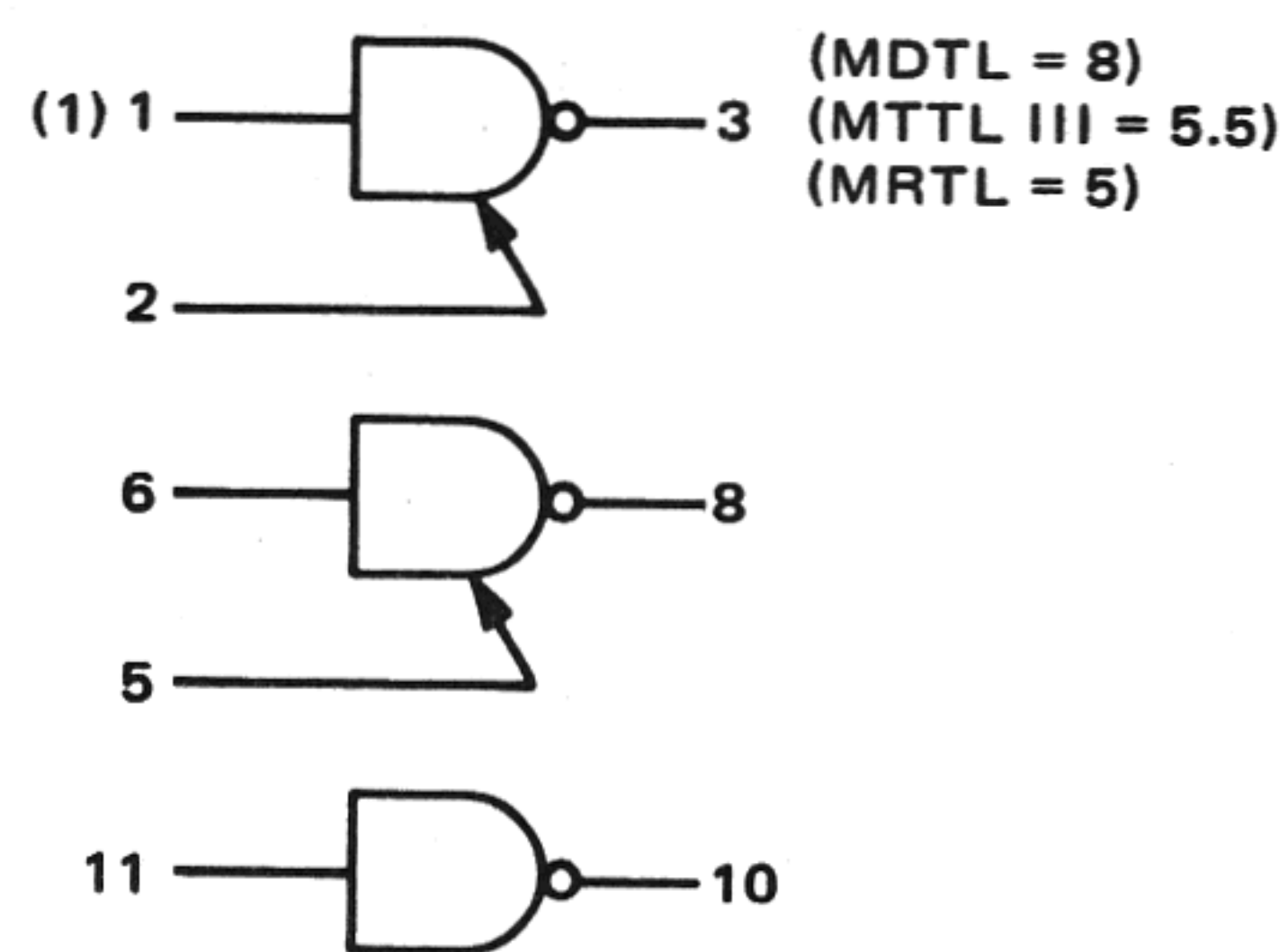
$$6 = 1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]$$

$t_{pd} = 140 \text{ ns typ}$
 $P_D = 180 \text{ mW typ/pkg (Inputs High)}$
 $26 \text{ mW typ/pkg (Input Low)}$

LOGIC DIAGRAMS (continued)

TRANSLATORS

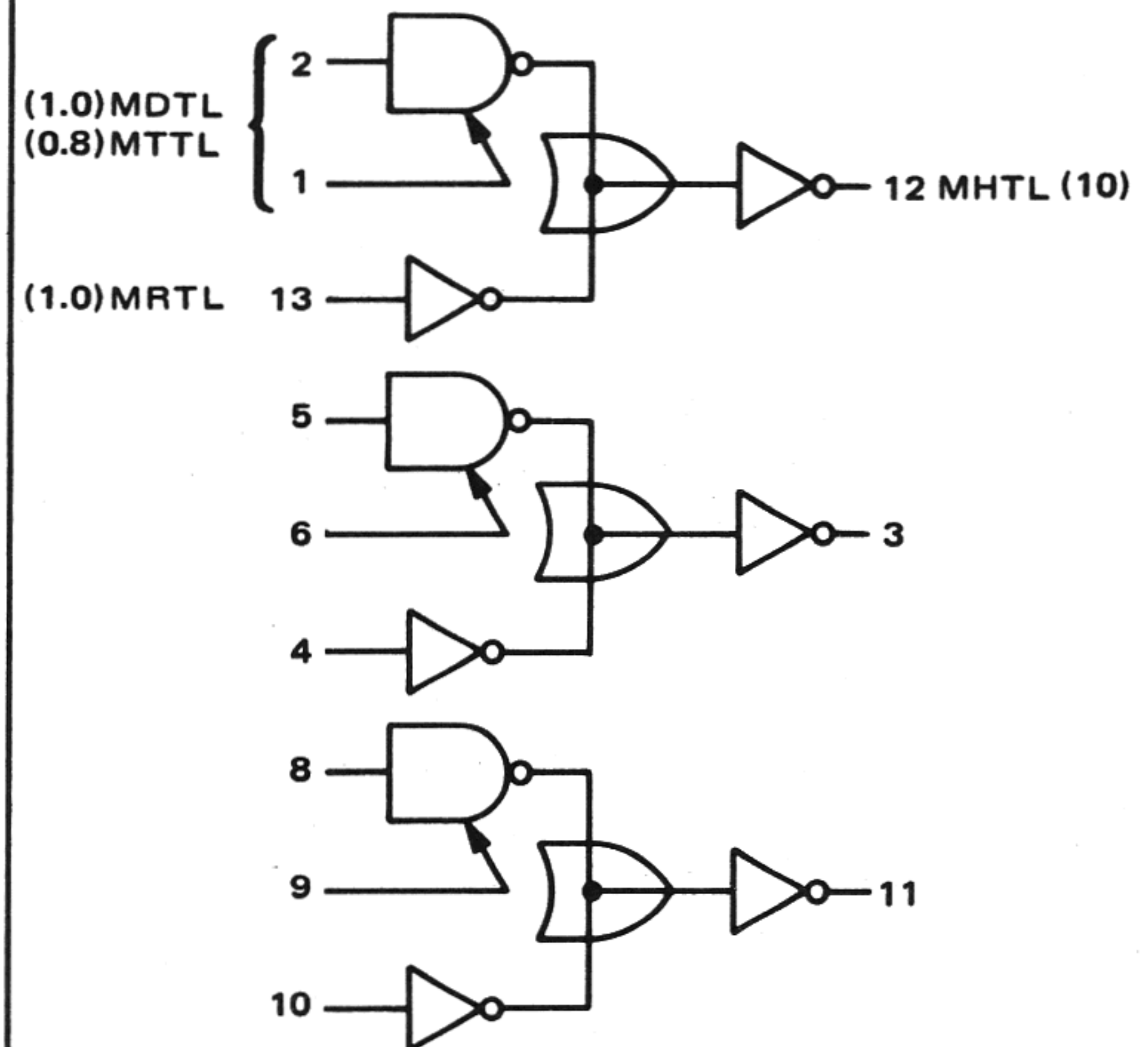
MC665
Triple Level Translator



$$3 = 1 \cdot [2]$$

$t_{pd} = 40 \text{ ns typ}$
 $P_D = 83 \text{ mW typ/pkg (DTL)}$
 $104 \text{ mW typ/pkg (RTL)}$

MC666
Triple Level Translator



$$12 = 2 \cdot [1] + 13$$

$t_{pd} = 75 \text{ ns typ}$
 $P_D = 105 \text{ mW typ/pkg}$