

SNx4HC175 Quadruple D-Type Flip-Flops With Clear

1 Features

- Wide operating voltage range of 2 V to 6 V
- Outputs can drive up to 10 LSTTL Loads
- Low power consumption, 80- μ A max I_{CC}
- Contain four flip-flops with double-rail outputs
- Typical $t_{pd} = 13$ ns
- ± 4 -mA output drive at 5 V
- Low input current of 1 μ A max

2 Applications

- Buffer/storage registers
- Shift registers
- Pattern generators

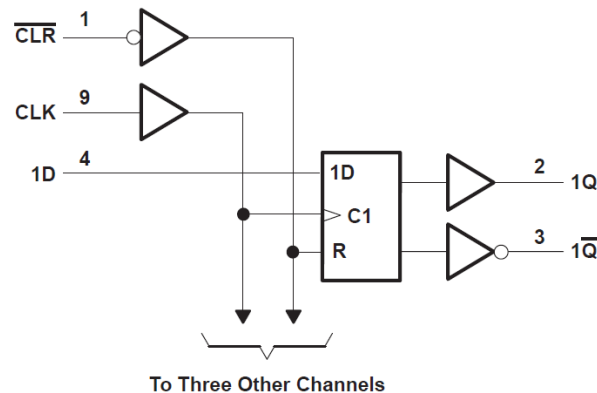
3 Description

These positive-edge-triggered D-type flip-flops have a direct clear ($\overline{CLR}$) input. The 'HC175 devices feature complementary outputs from each flip-flop.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN54HC175J	CDIP (16)	24.38 mm $\times$ 6.92 mm
SN74HC175D	SOIC (16)	9.90 mm $\times$ 3.90 mm
SN74HC175DBR	SSOP (16)	6.20 mm $\times$ 5.30 mm
SN74HC175N	PDIP (16)	19.31 mm $\times$ 6.35 mm
SN74HC175NSR	SO (16)	6.20 mm $\times$ 5.30 mm
SN74HC175PW	TSSOP (16)	5.00 mm $\times$ 4.40 mm
SNJ54HC175FK	LCCC (20)	8.89 mm $\times$ 8.45 mm
SNJ54HC175W	CFP (16)	10.16 mm $\times$ 6.73 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

Functional Block Diagram



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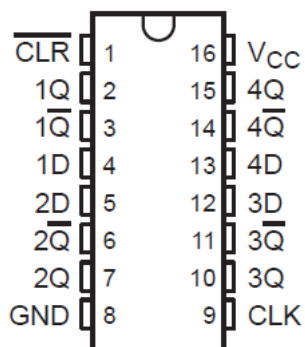
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4 Revision History

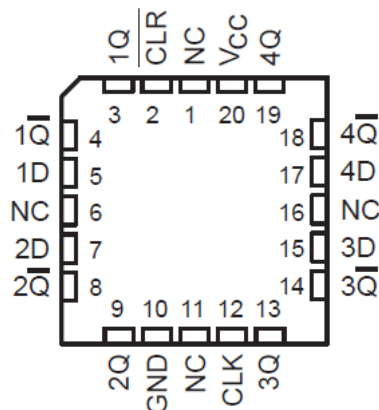
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2022) to Revision F (June 2022)	Page
Junction-to-ambient thermal resistance values increased. D was 73 is now 117.2, DB was 67 is now 102.7, N was 82 is now 60.5, NS was 64 is now 88.6, PW was 108 is now 137.5.....	4
Changes from Revision D (September 2003) to Revision E (February 2022)	Page
Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

5 Pin Configuration and Functions



J, W, D, DB, N, NS, or PW Package
16-Pin CDIP, CFP, SOIC, SSOP, PDIP, SO, or TSSOP
Top View



NC - No internal connection

FK Package
20-Pin LCCC
Top View

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
I_{IK}	Input clamp current ⁽²⁾	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Recommended Operating Conditions⁽¹⁾

			SN54HC175			SN74HC175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 6$ V	4.2			4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5			0.5	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 6$ V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition rise/fall time	$V_{CC} = 2$ V			1000			1000	ns
		$V_{CC} = 4.5$ V			500			500	
		$V_{CC} = 6$ V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.3 Thermal Information

		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
THERMAL METRIC		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	117.2	102.7	60.5	88.6	137.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.2	48.6	48	46.2	75.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.6	54.4	40.5	50.8	82.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	38.1	11.6	27.4	13.4	25.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	75.3	53.6	40.3	50.4	81.8	°C/W

6.3 Thermal Information (continued)

THERMAL METRIC		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC175		SN74HC175		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC} \text{ or } 0$		6 V		± 0.1	± 100		± 1000		± 1000	nA
I_{CC}	$V_I = V_{CC} \text{ or } 0, I_O = 0$		6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

6.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	$T_A = 25^\circ\text{C}$		SN54HC175		SN74HC175		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		4.2		5	MHz
			4.5 V		31		21		25	
			6 V		36		25		29	
t_w	Pulse duration	CLR low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK $\uparrow$	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLR inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		

6.5 Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	$T_A = 25^\circ\text{C}$		SN54HC175		SN74HC175		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_h	Hold time, data after CLK $\uparrow$	2 V	0		0		0		ns
		4.5 V	0		0		0		
		6 V	0		0		0		

6.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC175		SN74HC175		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	12		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{CLR}$	Any	2 V		52	150		255		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
	CLK	Any	2 V		58	150		255		190	
			4.5 V		16	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		38	75		110		90	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

6.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

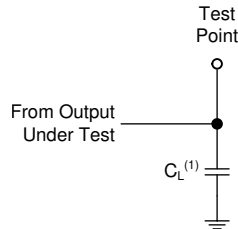
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	30	pF

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 7-1. Load Circuit for Push-Pull Outputs

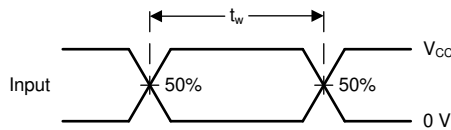


Figure 7-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

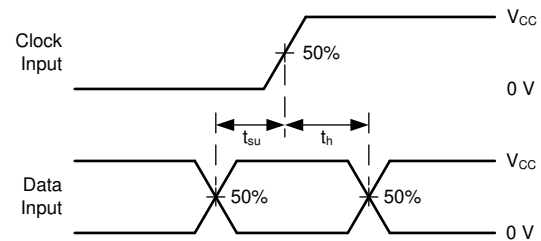
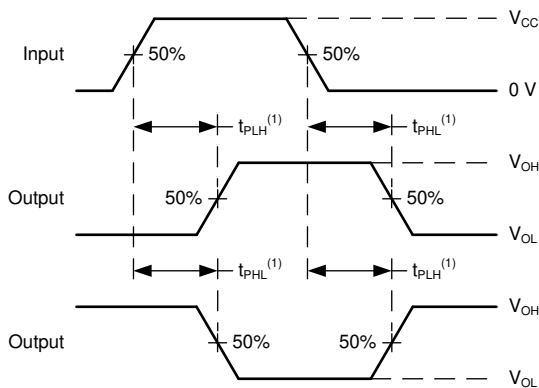
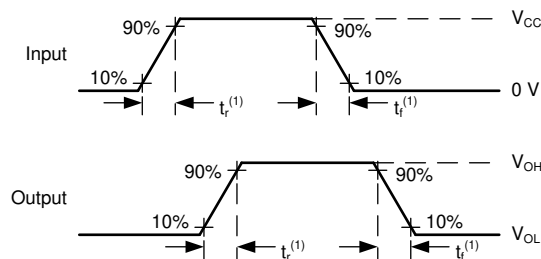


Figure 7-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 7-4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t .

Figure 7-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

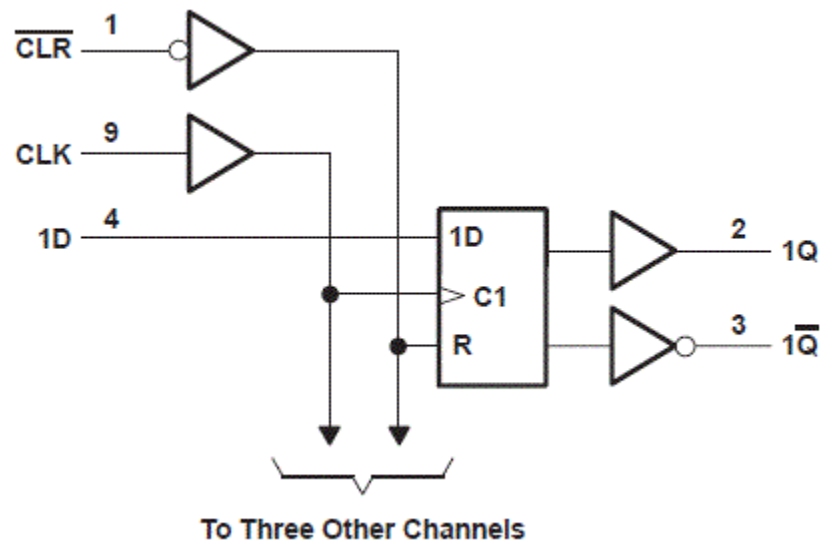
8 Detailed Description

8.1 Overview

These positive-edge-triggered D-type flip-flops have a direct clear ($\overline{\text{CLR}}$) input. The 'HC175 devices feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

8.3 Device Functional Modes

**Table 8-1. Function Table
(each flip-flop)**

INPUTS			OUTPUTS	
CLR	CLK	D	Q	$\overline{\text{Q}}$
L	X	X	L	H
H	$\uparrow$	H	H	L
H	$\uparrow$	L	L	H
H	L	X	Q_0	$\overline{\text{Q}}_0$

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

10 Layout

10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.