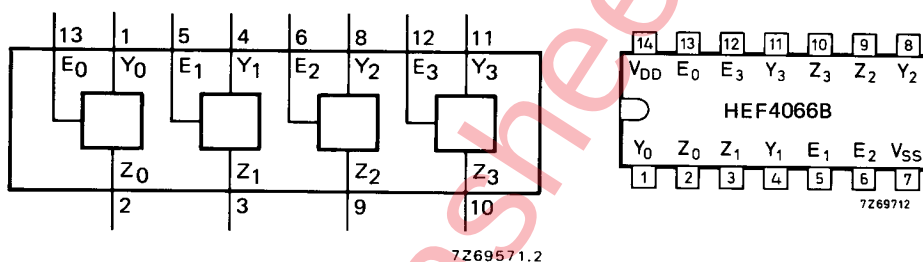


QUADRUPLE BILATERAL SWITCHES



The HEF4066B has four independent bilateral analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). When E is connected to V_{DD} a low impedance bidirectional path between Y and Z is established (ON condition). When E is connected to V_{SS} the switch is disabled and a high impedance between Y and Z is established (OFF condition).

The HEF4066B is pin compatible with the HEF4016B but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range.



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Fig. 2 Pinning diagram.

Fig. 1 Functional diagram.

PINNING

E_0 to E_3 enable inputs

Y_0 to Y_3 input/output terminals

Z_0 to Z_3 input/output terminals

HEF4066BP : 14-lead DIL; plastic (SOT-27).

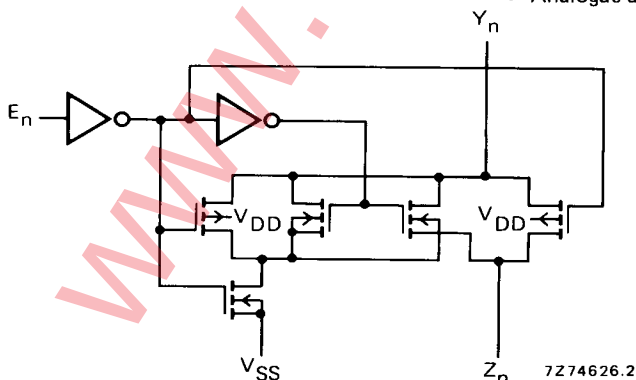
HEF4066BD : 14-lead DIL; ceramic (cerdip) (SOT-73).

HEF4066BT : 14-lead mini-pack; plastic
(SO-14; SOT-108A).

APPLICATION INFORMATION

An example of application for the HEF4066B is:

- Analogue and digital switching



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Fig. 3 Schematic diagram (one switch).



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Power dissipation per switch

P max. 100 mW

For other RATINGS see Family Specifications

D.C. CHARACTERISTICS

 $T_{amb} = 25^{\circ}\text{C}$

	V_{DD} V	symbol	min.	typ.	max.	conditions
ON resistance	5	R_{ON}	—	350	2500 Ω	E_n at V_{DD} $V_{is} = V_{SS}$ to V_{DD} see Fig. 4
	10		—	80	245 Ω	
	15		—	60	175 Ω	
ON resistance	5	R_{ON}	—	115	340 Ω	E_n at V_{DD} $V_{is} = V_{SS}$ see Fig. 4
	10		—	50	160 Ω	
	15		—	40	115 Ω	
ON resistance	5	R_{ON}	—	120	365 Ω	E_n at V_{DD} $V_{is} = V_{DD}$ see Fig. 4
	10		—	65	200 Ω	
	15		—	50	155 Ω	
' Δ ' ON resistance between any two channels	5	ΔR_{ON}	—	25	— Ω	E_n at V_{DD} $V_{is} = V_{SS}$ to V_{DD} see Fig. 4
	10		—	10	— Ω	
	15		—	5	— Ω	
OFF state leakage current, any channel OFF	5	I_{OZ}	—	—	— nA	E_n at V_{SS}
	10		—	—	— nA	
	15		—	—	200 nA	
E_n input voltage LOW	5	V_{IL}	—	2,25	1 V	$I_{is} = 10 \mu\text{A}$ see Fig. 9
	10		—	4,50	2 V	
	15		—	6,75	2 V	

	V_{DD} V	symbol	$T_{amb} (^{\circ}\text{C})$			conditions
			—40 max.	+25 max.	+85 max.	
Quiescent device current	5	I_{DD}	1,0	1,0	7,5 μA	$V_{SS} = 0$; all valid input combinations; $V_I = V_{SS}$ or V_{DD}
	10		2,0	2,0	15,0 μA	
	15		4,0	4,0	30,0 μA	
Input leakage current at E_n	15	$\pm I_{IN}$	—	300	1000 nA	E_n at V_{SS} or V_{DD}

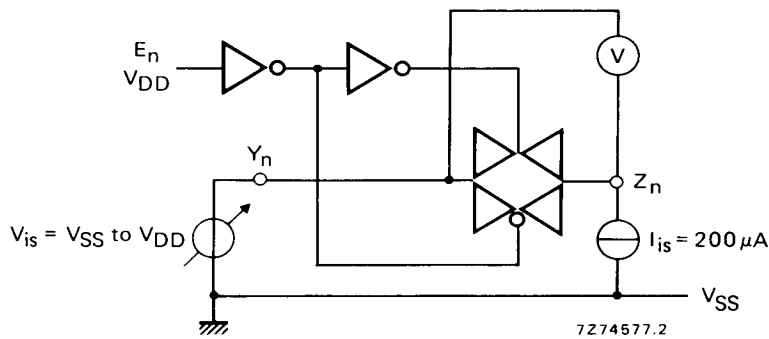


Fig. 4 Test set-up for measuring R_{ON} .

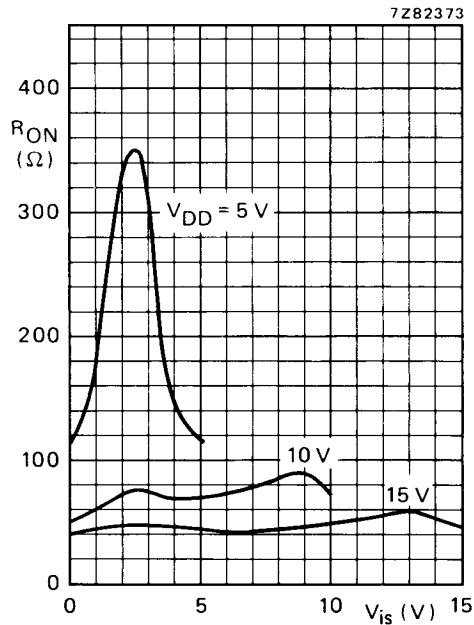


Fig. 5 Typical R_{ON} as a function of input voltage.

E_n at V_{DD}
 $I_{is} = 200 \mu A$
 $V_{SS} = 0 V$

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS} .

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V _{DD} V	symbol	typ.	max.		
Propagation delays V _{is} → V _{os} HIGH to LOW	5	t _{PHL}	10	20	ns	} note 1
	10		5	10	ns	
	15		5	10	ns	
LOW to HIGH	5	t _{PLH}	10	20	ns	} note 1
	10		5	10	ns	
	15		5	10	ns	
Output disable times E _n → V _{os} HIGH	5	t _{PHZ}	80	160	ns	} note 2
	10		65	130	ns	
	15		60	120	ns	
LOW	5	t _{PLZ}	80	160	ns	} note 2
	10		70	140	ns	
	15		70	140	ns	
Output enable times E _n → V _{os} HIGH	5	t _{PZH}	40	80	ns	} note 2
	10		20	40	ns	
	15		15	30	ns	
LOW	5	t _{PZL}	45	90	ns	} note 2
	10		20	40	ns	
	15		15	30	ns	
Distortion, sine-wave response	5		0,25		%	} note 3
	10		0,04		%	
	15		0,04		%	
Crosstalk between any two channels	5		—		MHz	} note 4
	10		1		MHz	
	15		—		MHz	
Crosstalk; enable input to output	5		—		mV	} note 5
	10		50		mV	
	15		—		mV	
OFF-state feed-through	5		—		MHz	} note 6
	10		1		MHz	
	15		—		MHz	
ON-state frequency response	5		—		MHz	} note 7
	10		90		MHz	
	15		—		MHz	

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	800 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	3 500 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	10 100 f _i + Σ(f _o C _L) × V _{DD} ²	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.

V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10\text{ k}\Omega$ to V_{SS} ; $C_L = 50\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$; $V_{is} = V_{DD}$ (square-wave); see Figs 6 and 10.

2. $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$ (square-wave);

$V_{is} = V_{DD}$ and R_L to V_{SS} for t_{PHZ} and t_{PZH} ;

$V_{is} = V_{SS}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL} ; see Figs 6 and 11.

3. $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; $E_n = V_{DD}$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $f_{is} = 1\text{ kHz}$; see Fig. 7.

4. $R_L = 1\text{ k}\Omega$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);

$20 \log \frac{V_{os(B)}}{V_{is(A)}} = -50\text{ dB}$; $E_n(A) = V_{SS}$; $E_n(B) = V_{DD}$; see Fig. 8.

5. $R_L = 10\text{ k}\Omega$ to V_{SS} ; $C_L = 15\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 6.

6. $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; $E_n = V_{SS}$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);

$20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 7.

7. $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; $E_n = V_{DD}$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);

$20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$; see Fig. 7.

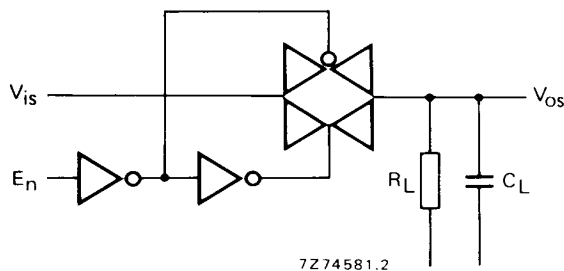


Fig. 6.

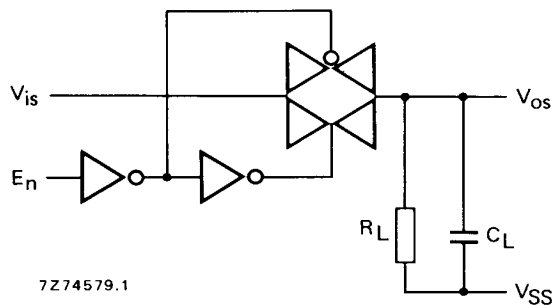


Fig. 7.

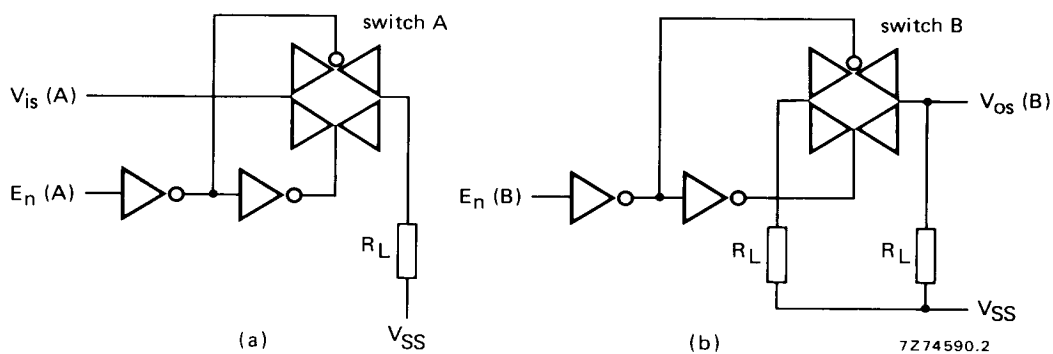


Fig. 8.

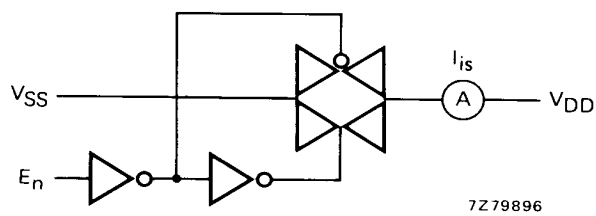


Fig. 9.

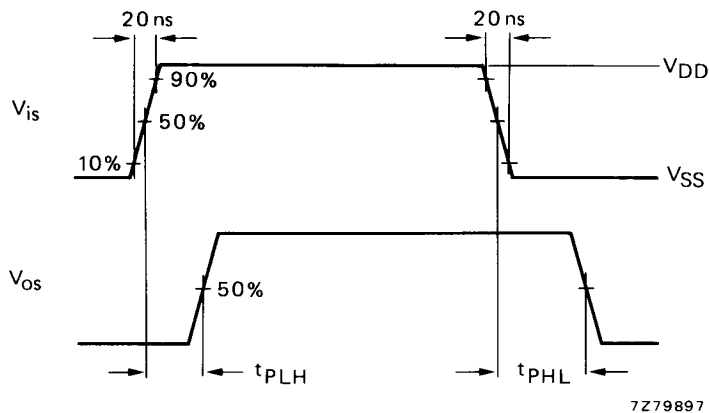
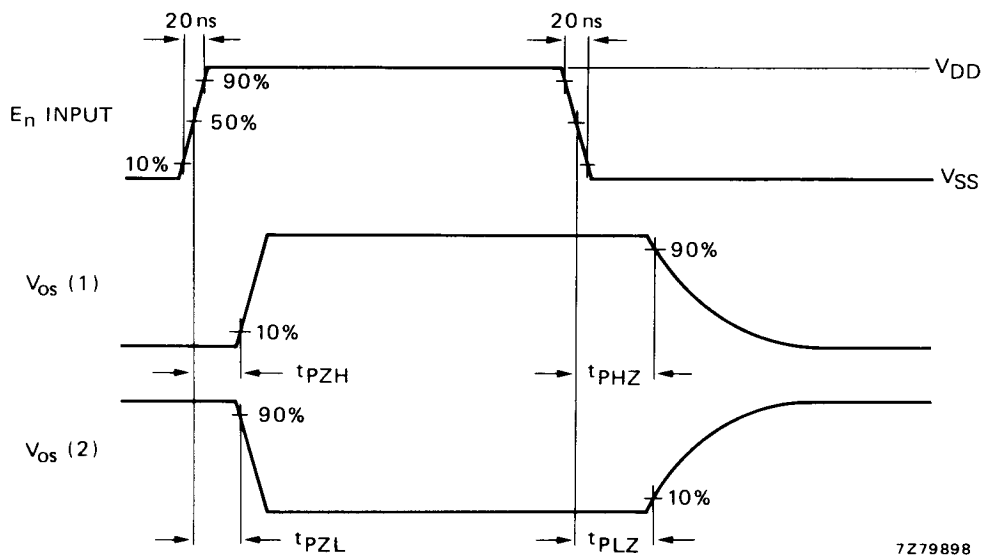


Fig. 10 Waveforms showing propagation delays from V_{is} to V_{os} .



(1) V_{is} at V_{DD} ; (2) V_{is} at V_{SS} .

Fig. 11 Waveforms showing output disable and enable times.